



Measuring Performance of Embedded Capacitance Layers

John Andresakis

10/23/2007

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mitsui kinzoku corporate group





Overview

- Sanmina/Sun Microsystems Testing
- Toshiba Study
 - Background
 - Test Panel Design
 - Electrical Results
 - Summary
- (NCR) Teradata Study
 - Project Team Formation
 - Design Review/Product Build
 - Electrical Performance
 - Cost/Benefit Analysis
 - Future Studies/Lessons Learned
 - Summary
- Discrete Embedded Capacitors

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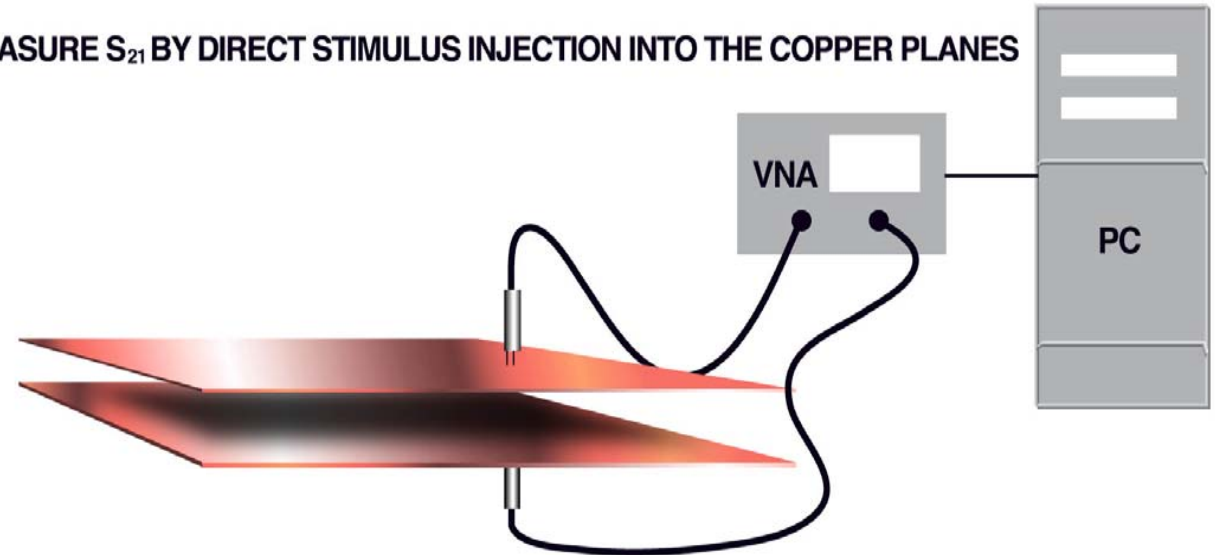




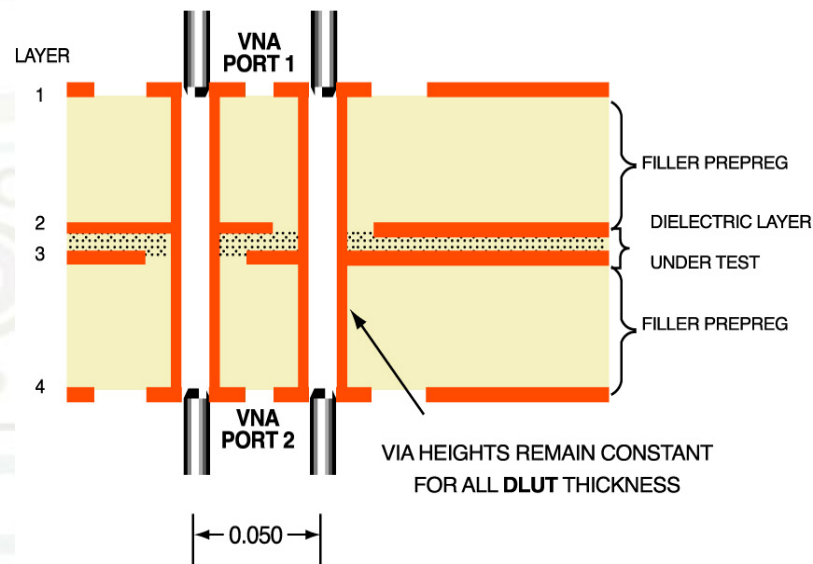
PCB Electrical Performance

Sanmina/Sun Test Vehicle

MEASURE S_{21} BY DIRECT STIMULUS INJECTION INTO THE COPPER PLANES



4 LAYER TEST BOARD CROSS SECTION VIEW



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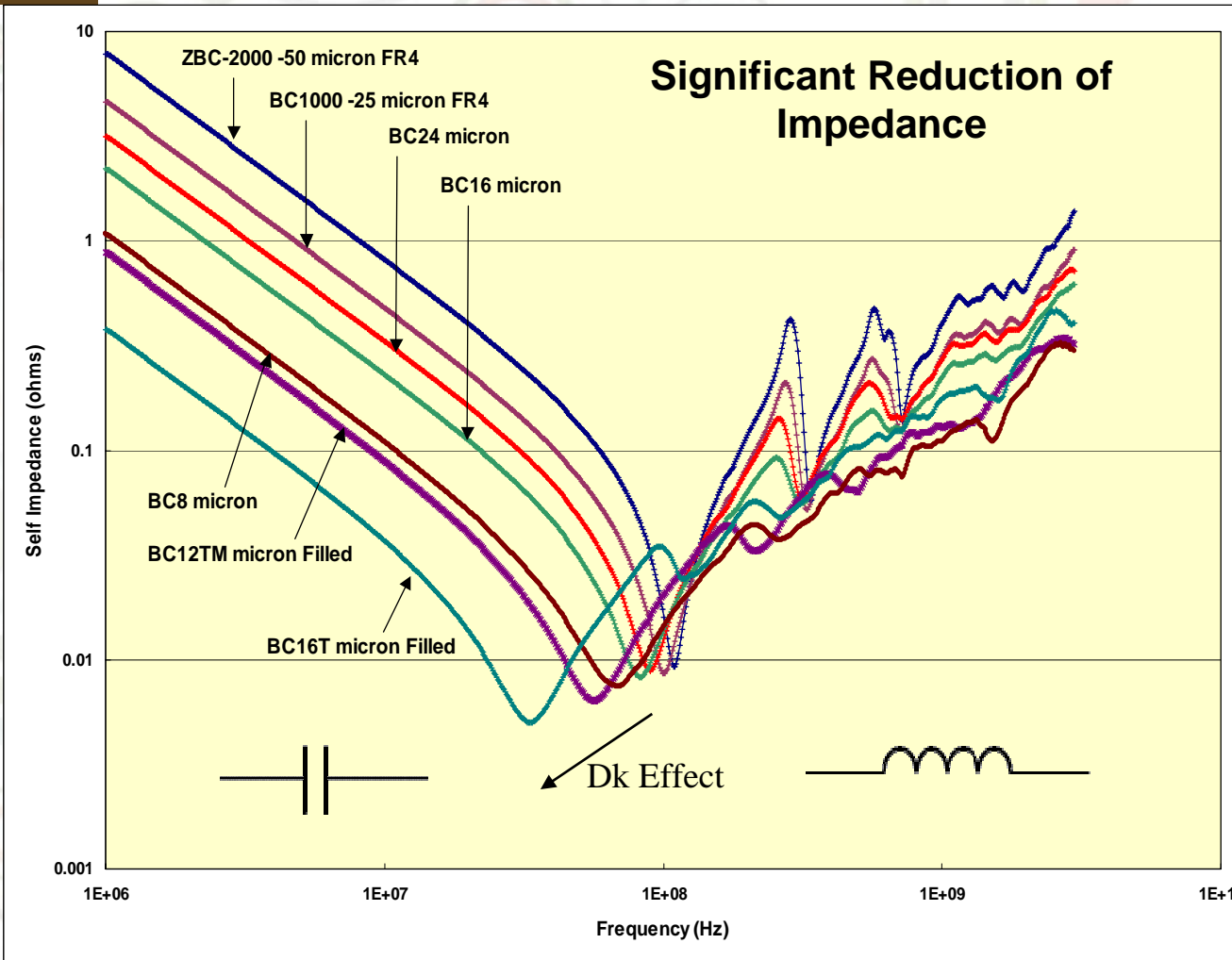




PCB Electrical Performance

Sanmina/Sun Test Vehicle

Panel Size= 50 in²
80% Retained Cu



Product	nF
ZBC2000	16
ZBC1000	32
BC24	40
BC16	64
BC12	76
BC8	124
BC12TM	180
BC16T	440

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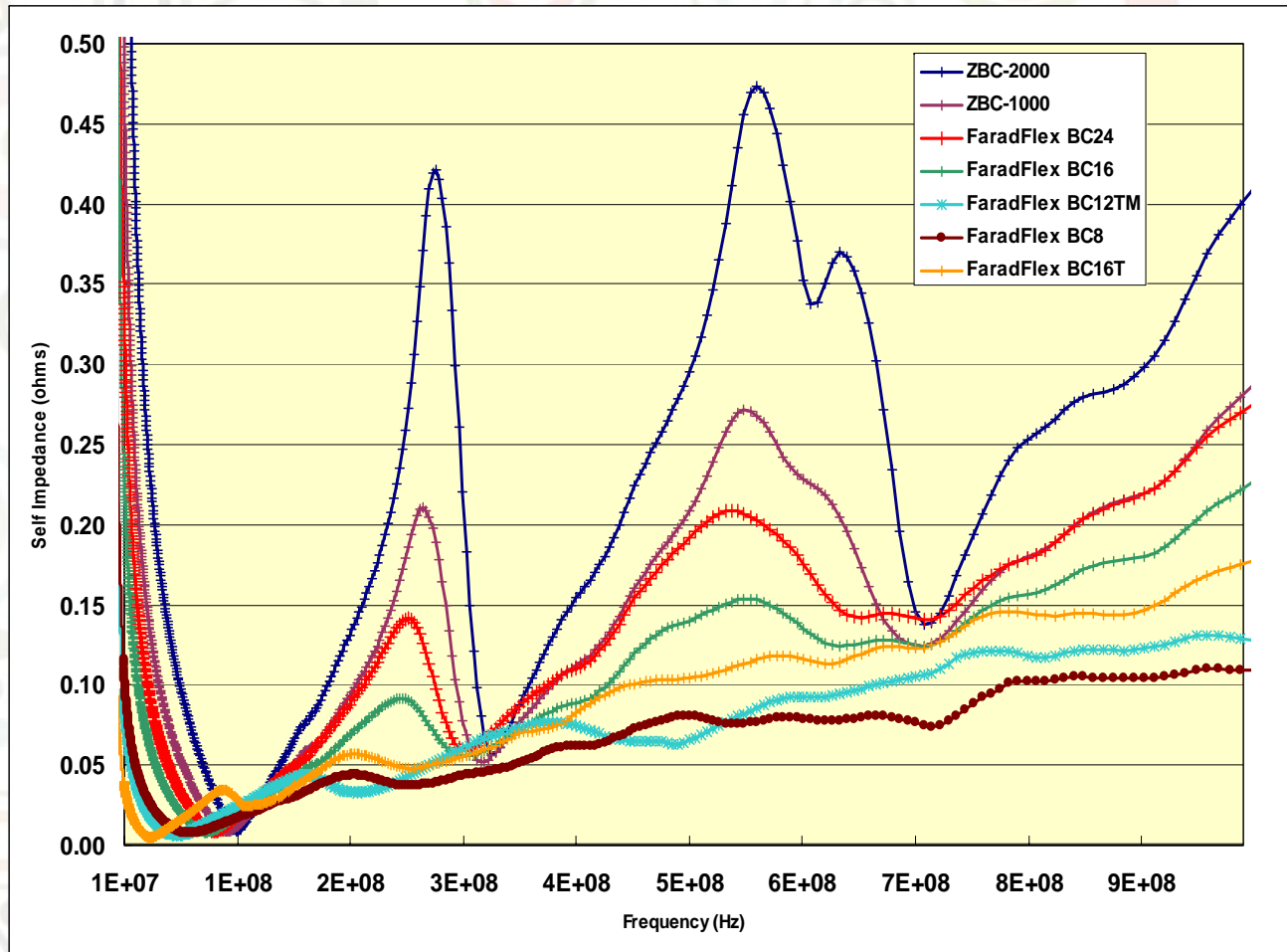


PCB Electrical Performance

Sanmina/Sun Test Vehicle

(Up to 1 GHz)

Panel Size= 50 in²
80% Retained Cu



Product	nF
ZBC2000	16
ZBC1000	32
BC24	40
BC16	64
BC12	76
BC8	124
BC12TM	180
BC16T	440

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Project Team

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Corporate Manufacturing Engineering Center
Toshiba Corporation, Japan

John Andresakis, Kazuhiro Yamazaki
Oak-Mitsui Technologies

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Background

- **Clock speed of high-speed digital circuits is becoming faster year by year.**
- **High-speed interface circuits are already exceeding 1Gbps, and approaching 10Gbps.**
- **Power bus structure in a high-speed printed circuit board (PCB) is an important design parameter**
 - **for mitigating reference voltage fluctuation caused by the transient current of active ICs.**
 - **for reducing radiating emission due to PCB's antenna property.**

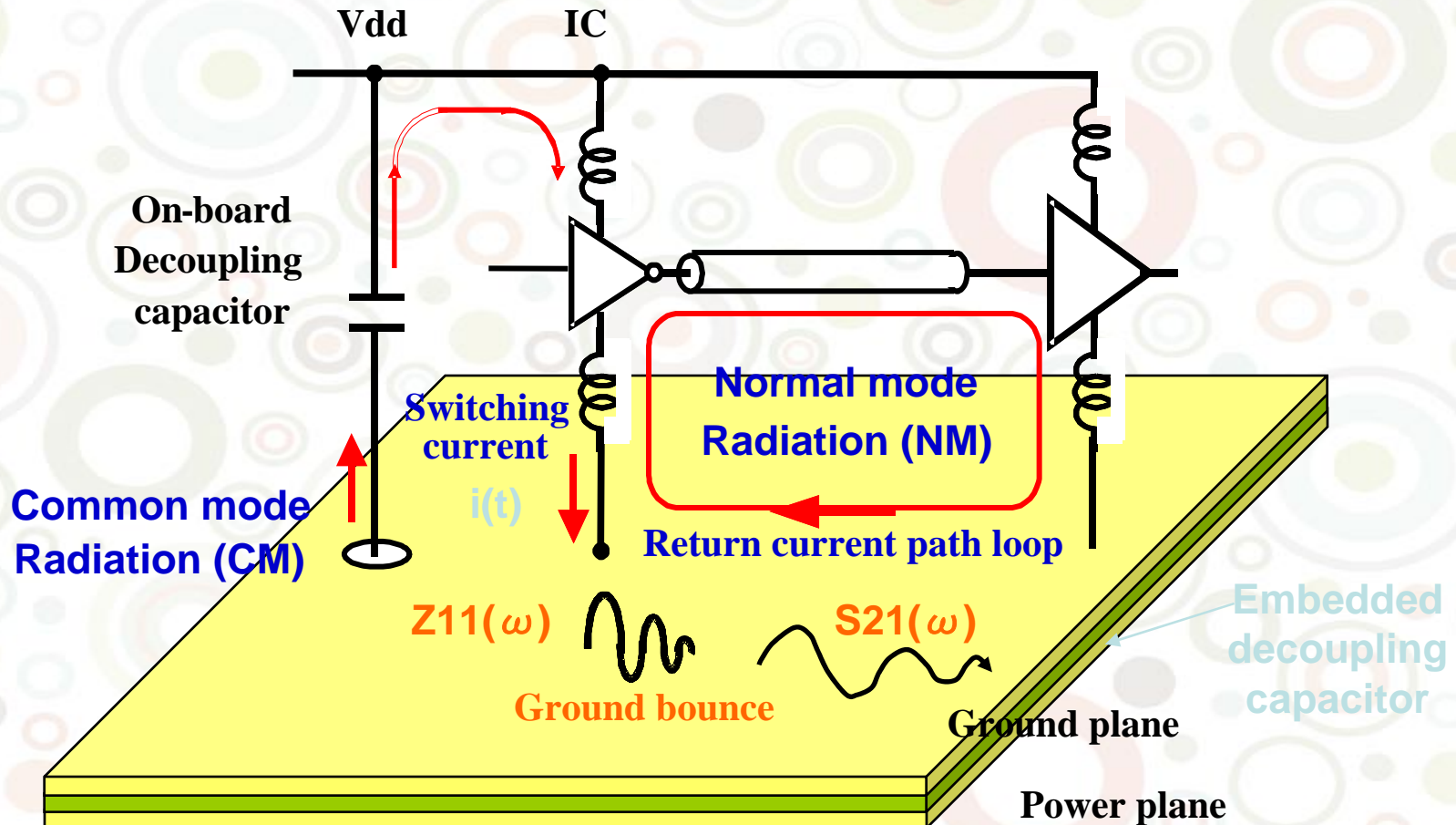
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Major EMI sources in a PCB

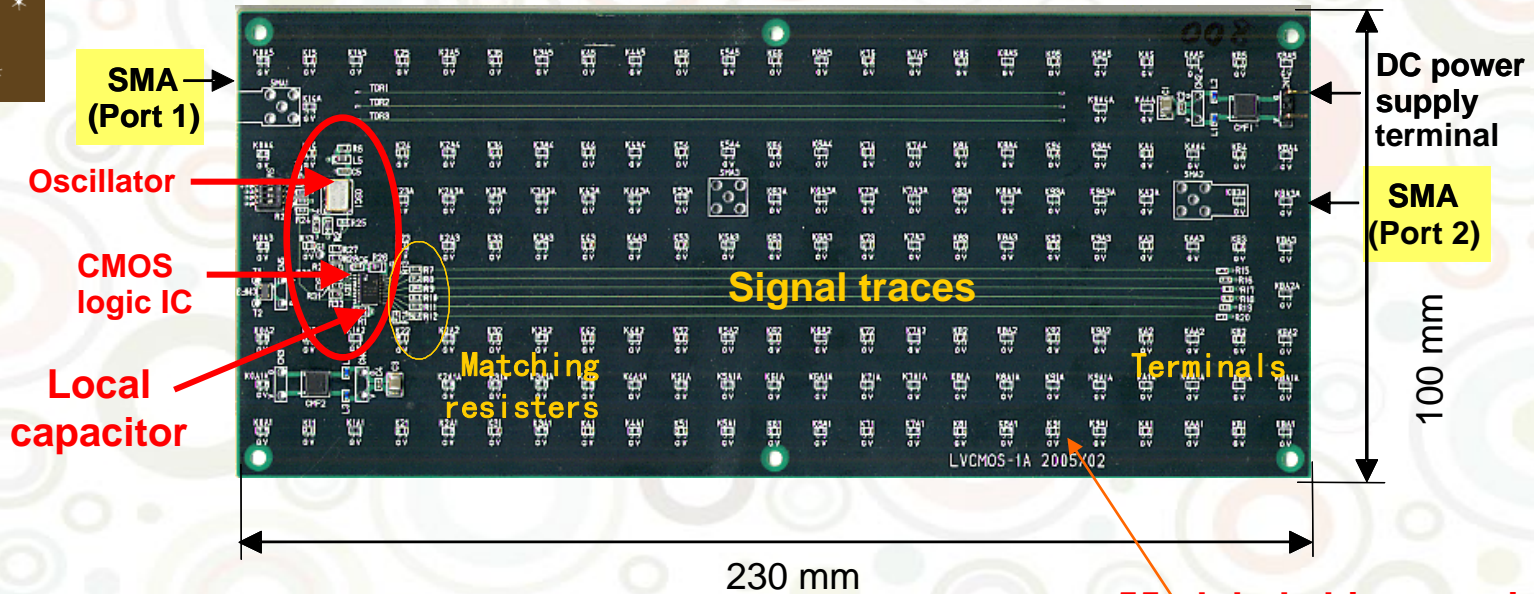


- Two major EMI sources; one is NM radiation by signal return path loop, and the other is CM radiation excited by IC' switching current .
- Insulator thickness determines the power supply impedance, and the antenna property of PCB.

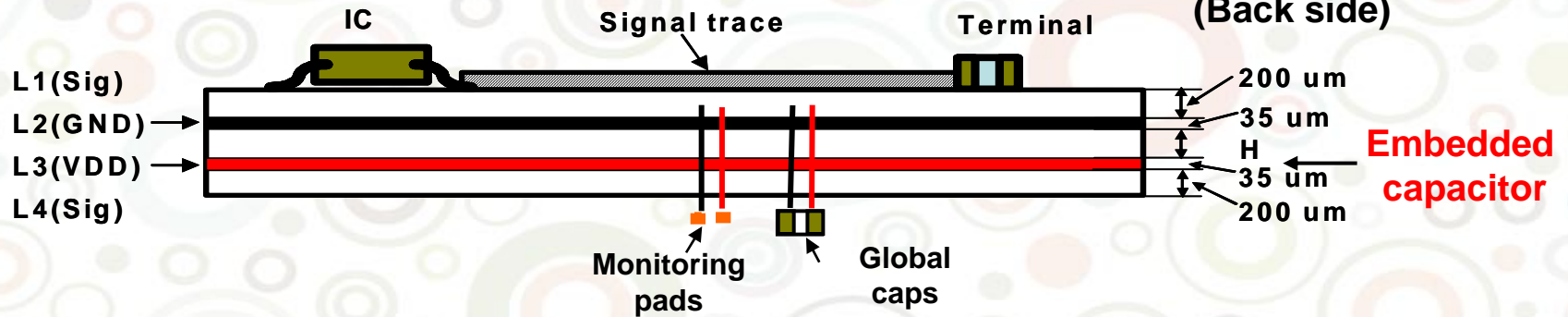
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Evaluation board outline

Front side view



Cross-sectional view

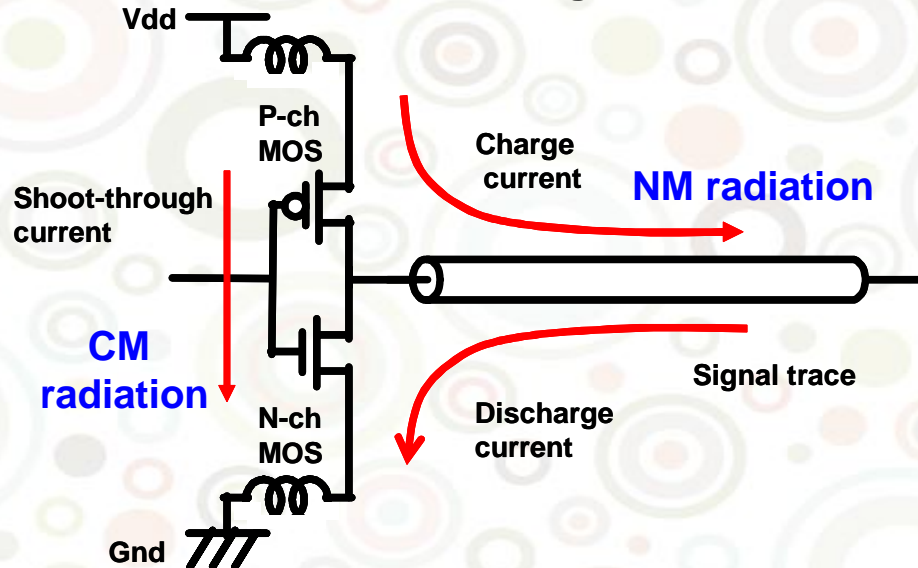
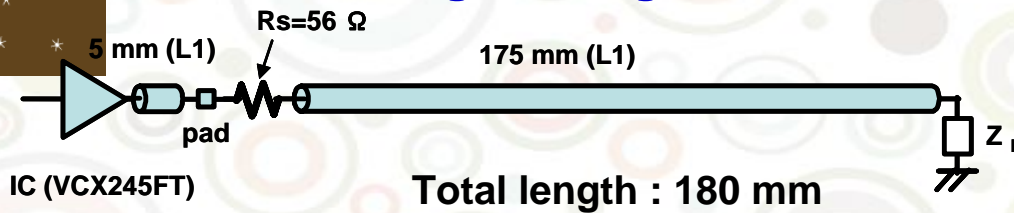


**55 global chip capacitors
(0.1 μF , 5 \times 11)
(Back side)**

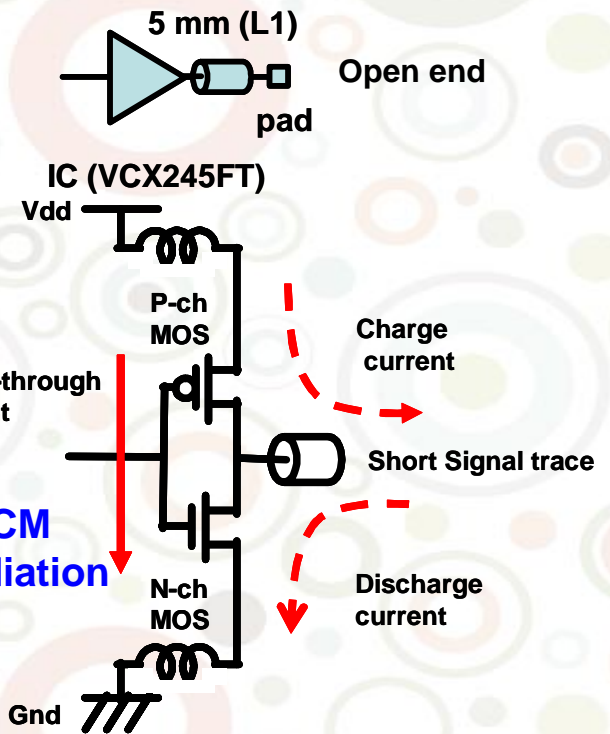
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Long and short signal routings

Long routing



Short routing



- Two signal routings with different lengths were prepared to distinguish CM radiation of power bus from NM radiation of signal line.
- Long routing excites NM radiation by charge current together with CM mode.
- Short routing mainly excites CM radiation by shoot-through current of IC.

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Parameters of evaluation boards

1) Insulator thicknesses between L2 and L3

	Dielectric thickness (H)	Dielectric constant(Er)
FR4-200	200	4.4
FR4-100	100 (um)	4.4
FR4-50	50	4.4
BC16	16	4.4
BC8	8	4.4
BC16T	16	30

Conventional

Embedded decoupling capacitor

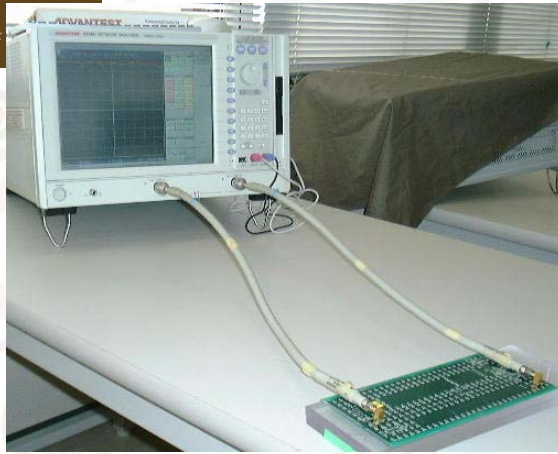
2) Discrete global chip capacitors

- Two types of assembled board without or with global chip capacitors.

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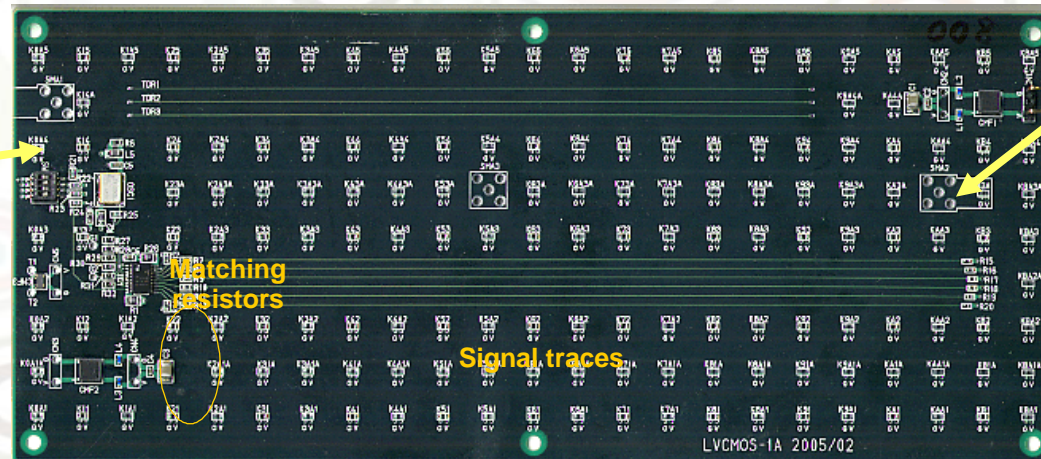
S parameter measurement



VNA : Agilent 8720D
: 50MHz~2GHz

Port 1
SMA
connector

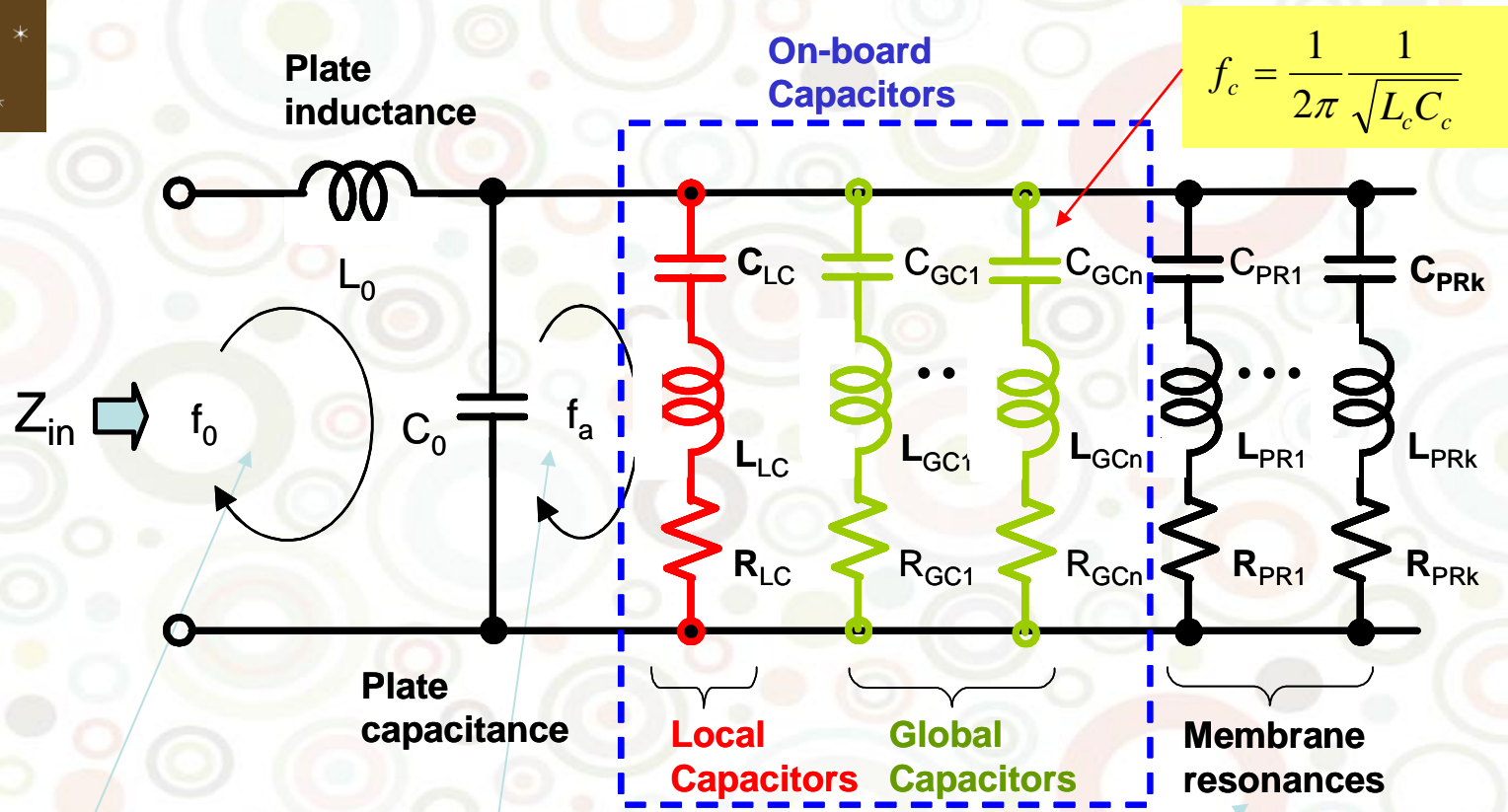
Port 2
SMA
connector



- without or with global chip capacitors

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Lumped circuit model of power/ground plane



$$f_0 = \frac{1}{2\pi} \frac{1}{\sqrt{L_0 C_0}}$$

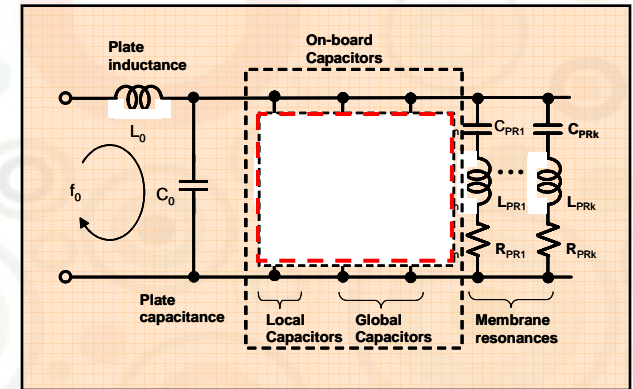
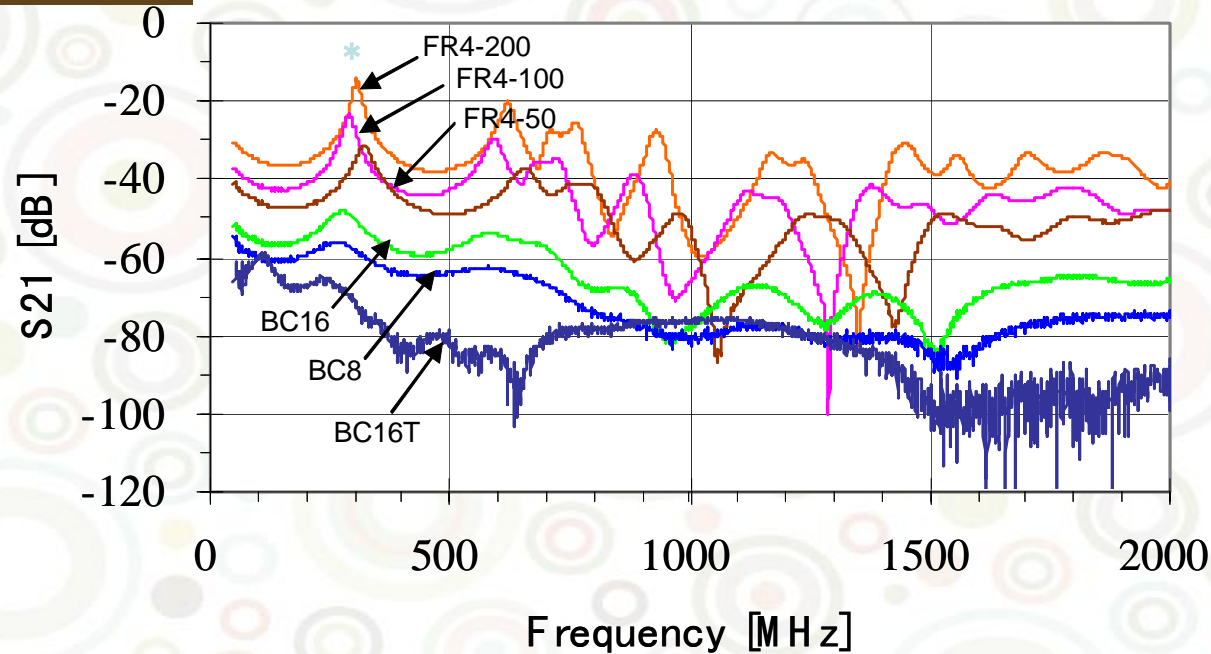
$$f_a = \frac{1}{2\pi} \frac{1}{\sqrt{L_{LC} (C_0 + C_{LC})}}$$

$$f_{(m,n)} = \frac{v_0}{2\sqrt{\epsilon_r}} \sqrt{\left(\frac{m}{a}\right)^2 + \left(\frac{n}{b}\right)^2}$$

- There are 4 major resonances in the power bus structures.
- Parallel resonance f_a becomes prominent without global capacitors.

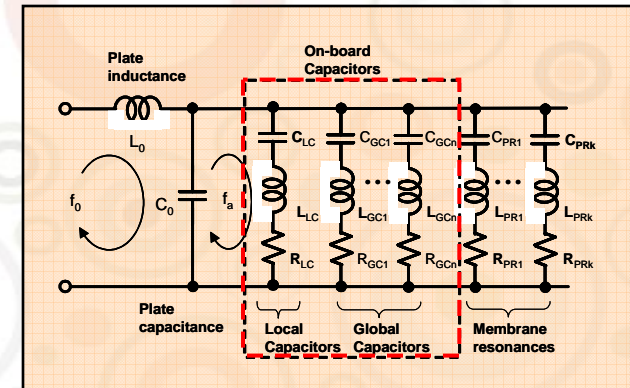
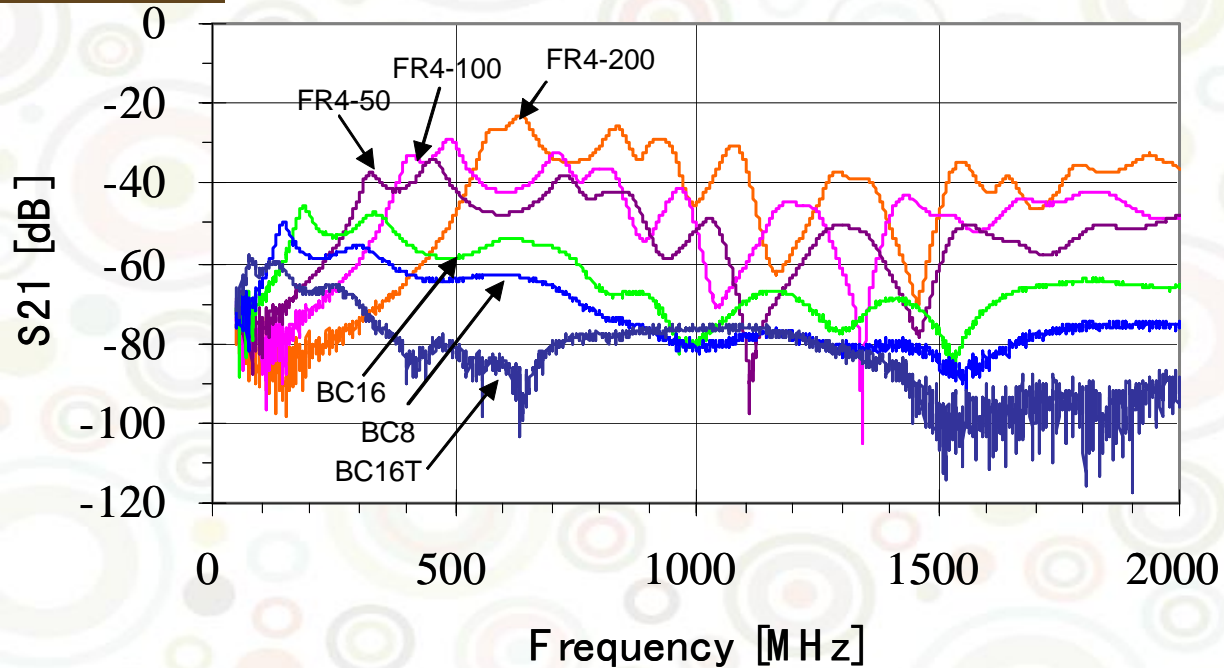
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Measured S21 without any on-board capacitors



- S21 values of power bus became lower over the wide frequency range by thinner insulators of embedded decoupling capacitor.
- Resonance peaks can be suppressed for the thicknesses below 16 μm .

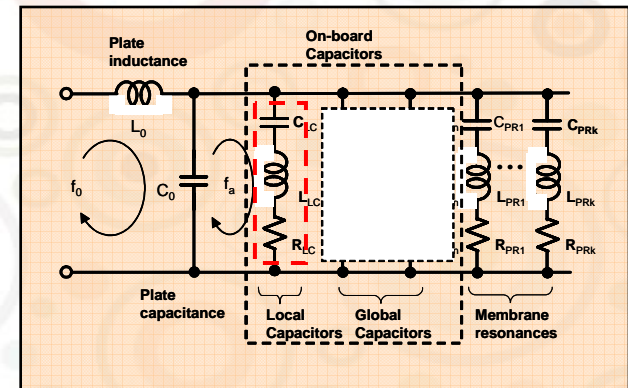
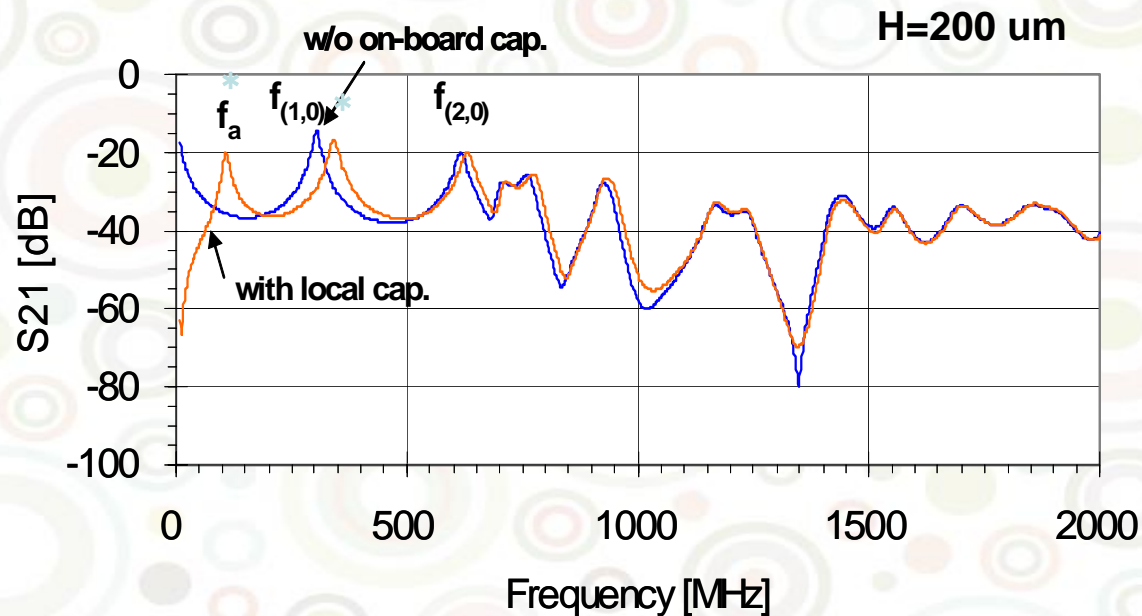
Measured S21 with on-board capacitors



- Global capacitors affected only to the low frequency region of S21, but made extremely low value from DC to a certain frequency.
- Contrary to the expectation, this frequency region with low S21 value became broader for the PCB with thicker insulator.

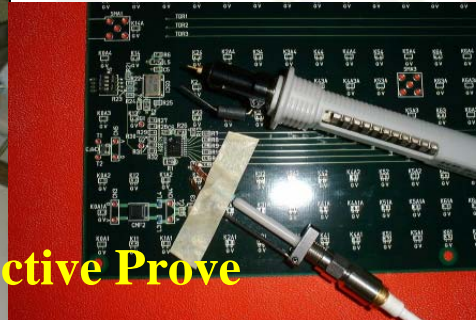
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Measured S21 only with local capacitors



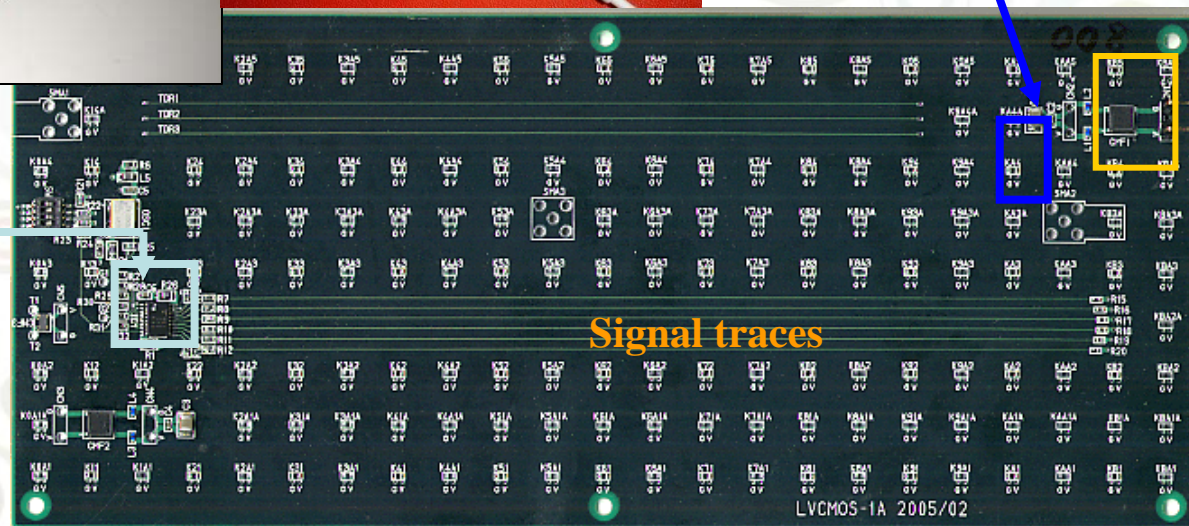
- In the case without global capacitors, parallel resonance (f_a) caused by the combination of plate capacitor and local capacitor becomes prominent.

Ground bounce Measurement



Close point to P/S
(V G b)
DC P/S
terminal

Nearest point
to IC (V G a)



- Ground bounce can be measured at the monitoring pads on the whole area of PCB.
- Ground bounce is defined as the voltage difference between pwr/gnd planes.

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Ground bounce comparison for two thicknesses excited by short trace

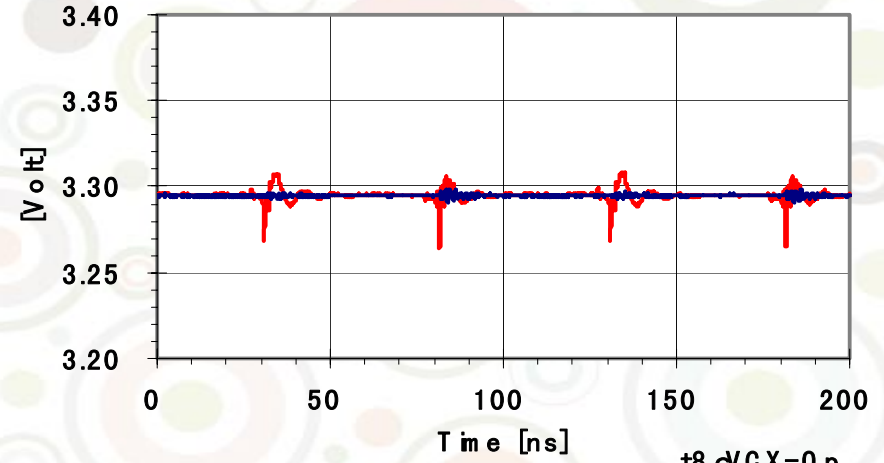
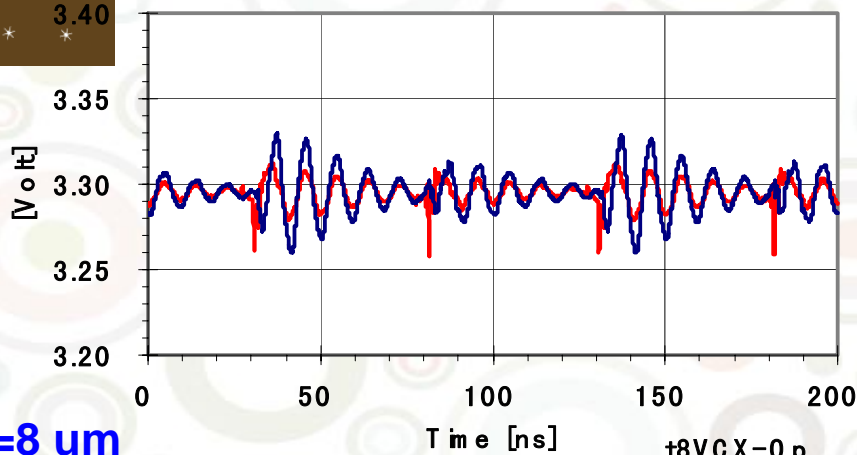
without global caps

with global caps

H=200 um

t200VCX-0 p

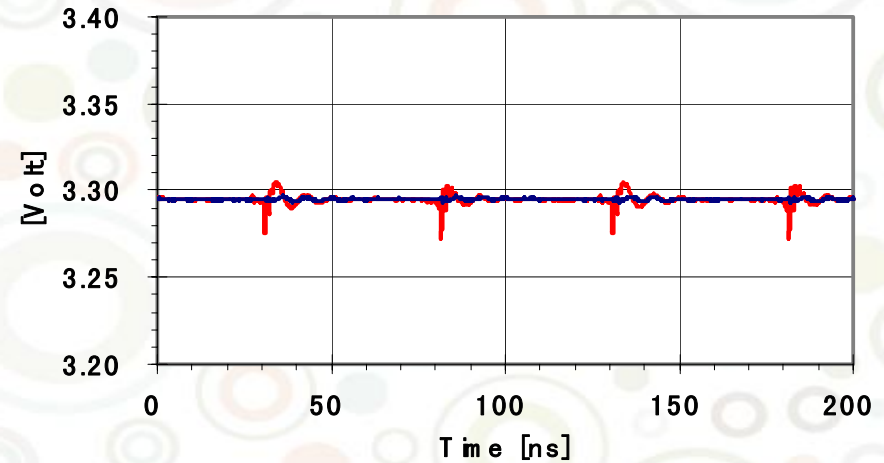
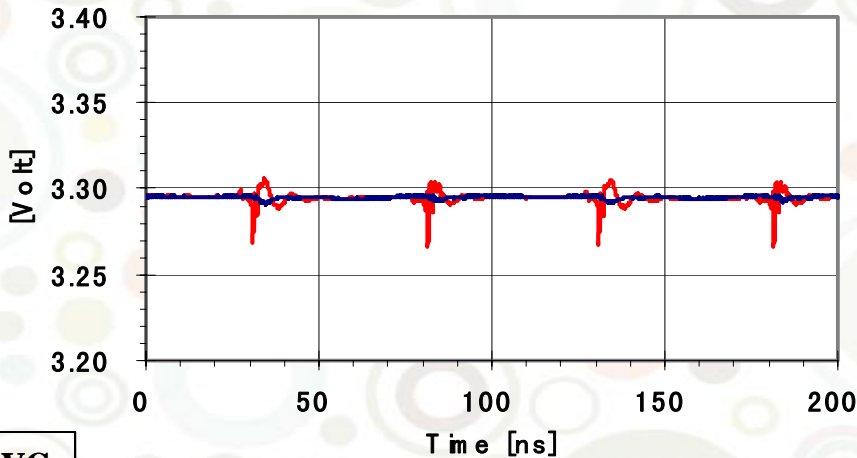
t200cVCX-0 p



H=8 um

t8VCX-0 p

t8 cVCX-0 p



- Large ground bounce were measured without global caps for thick insulator.
- Ground bounces at VGb were greatly reduced by thin embedded cap, or global caps.

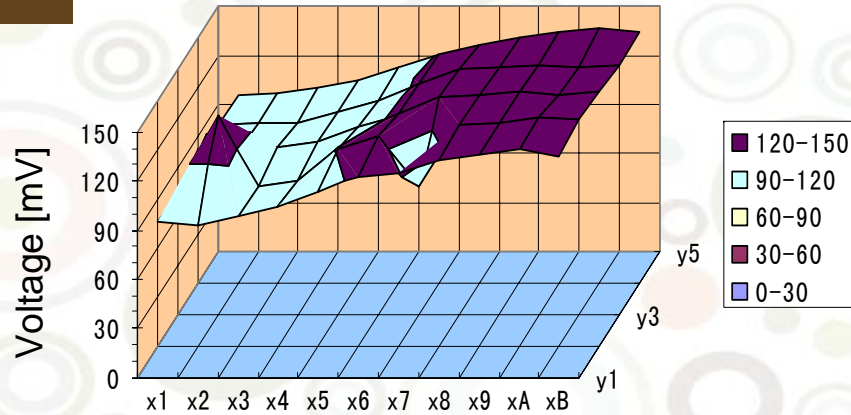
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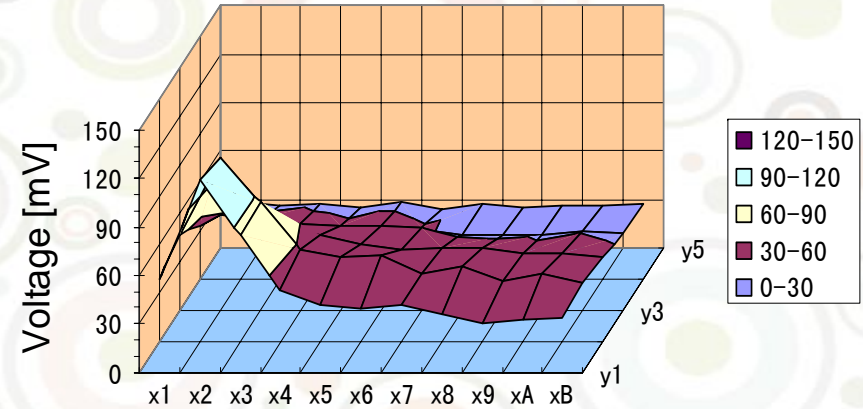


Ground bounce distribution in the whole area

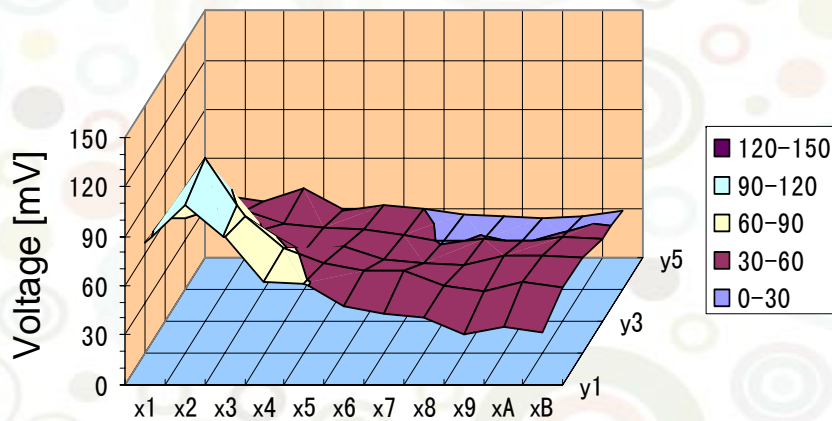
H=200 um without global caps



H=8 um without global caps



H=200 um with global caps



- Both thin embedded cap and global caps were effective to reduce noise.
- Thin insulator was slightly more effective for reducing noise than global caps.

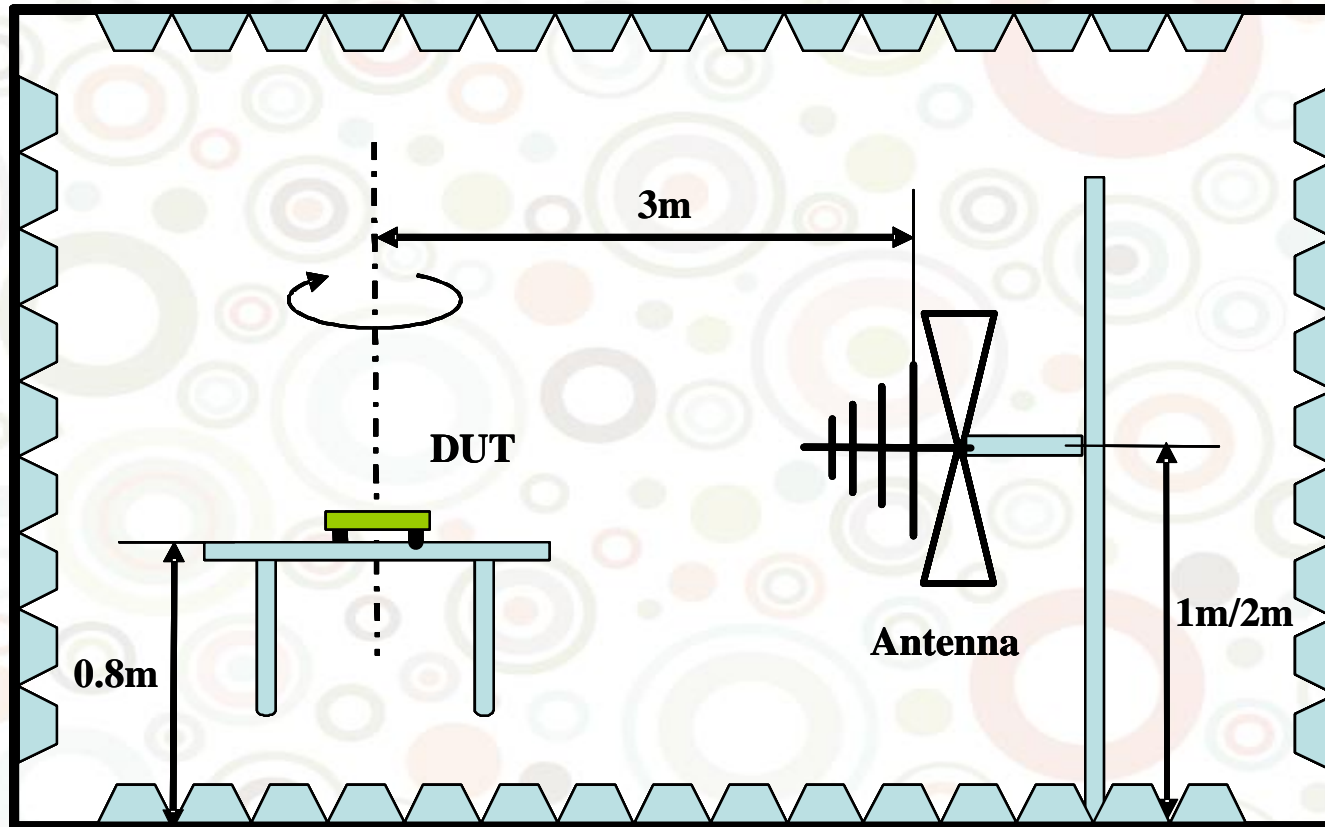
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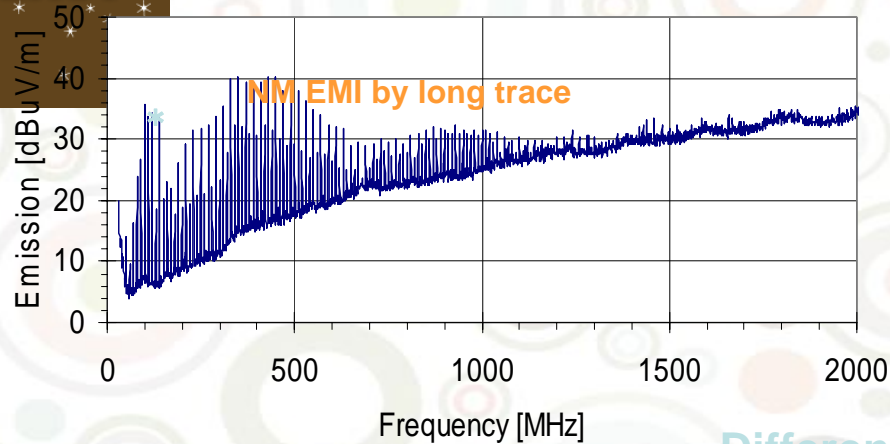
Far-field measurement set-up



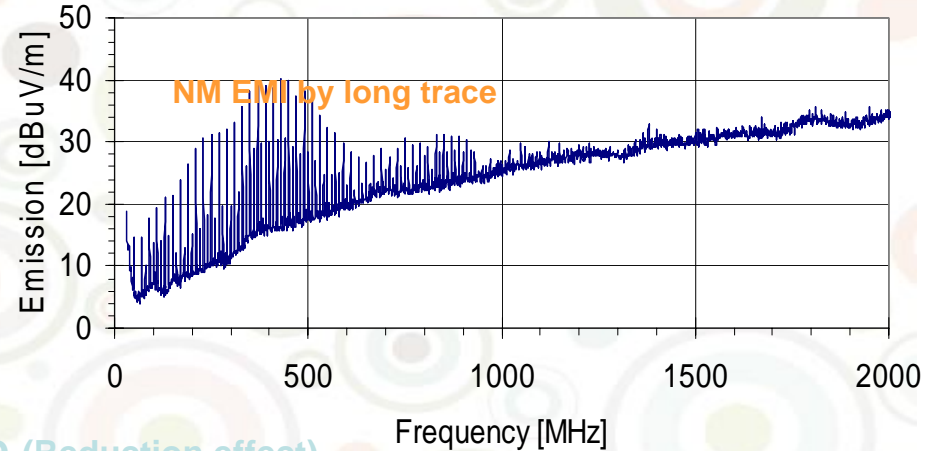
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Reduction of radiated emission by embedded capacitor excited by long traces

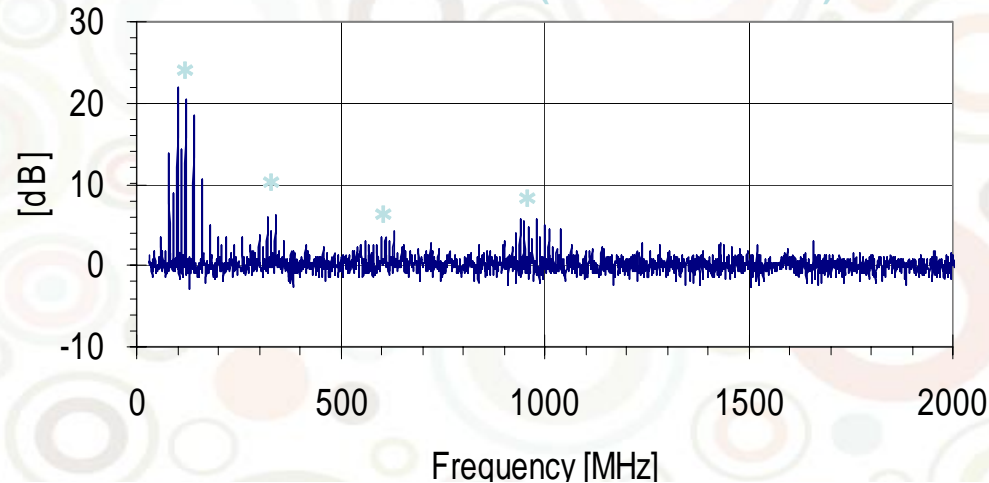
H= 200 um



H= 8 um



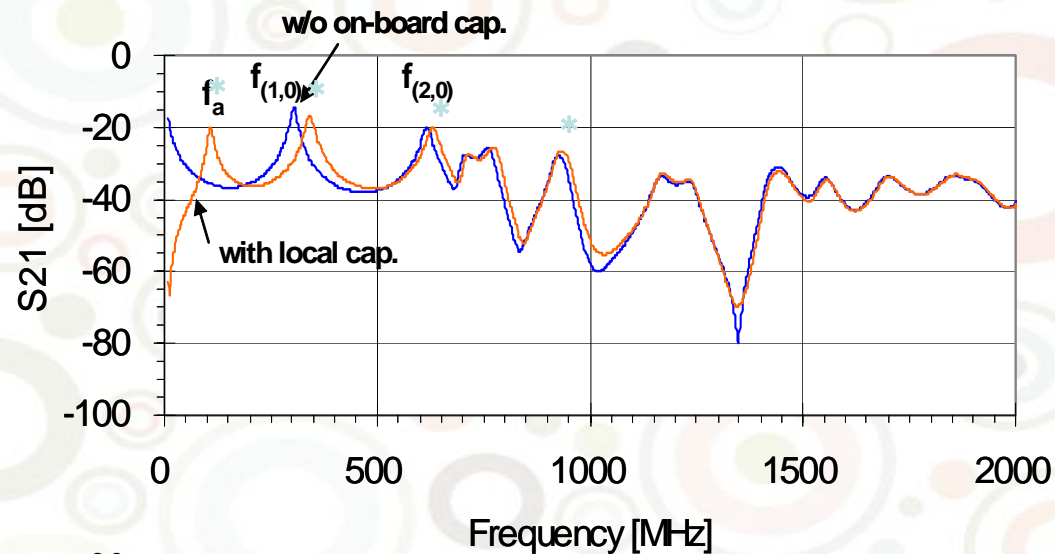
Difference (Reduction effect)



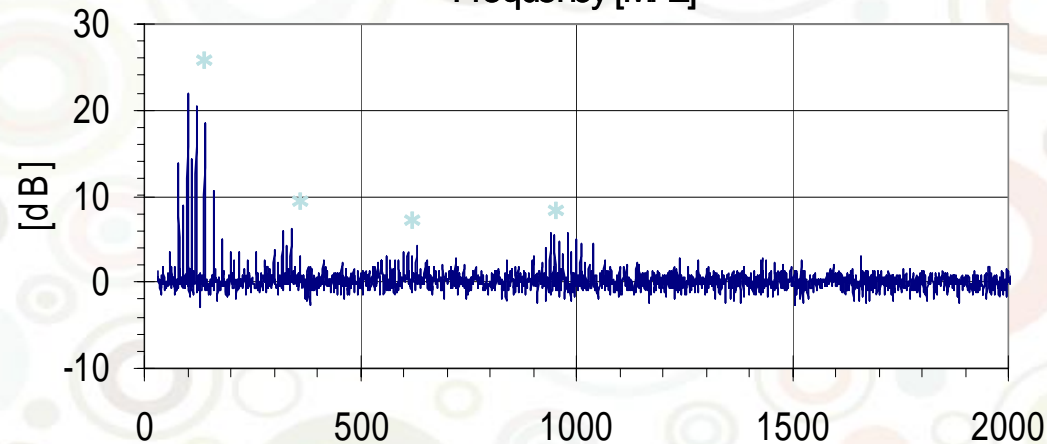
- High level of reduction was observed at the frequencies corresponding to the resonant frequencies in S21 property.
- Embedded capacitor did not affect NM radiation for the L1 routing.

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Correlation between S21 and CM radiation



H=200 μ m



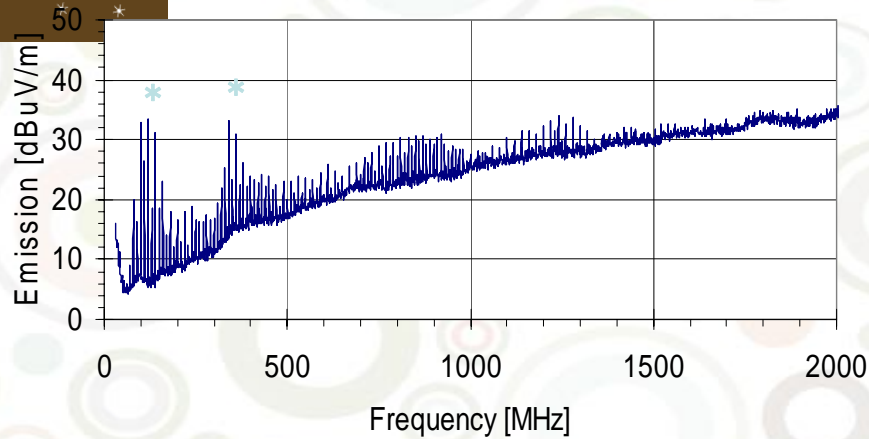
- Frequencies with high CM radiation were well correlated to peak frequencies of S21 by taking a local capacitor into account.

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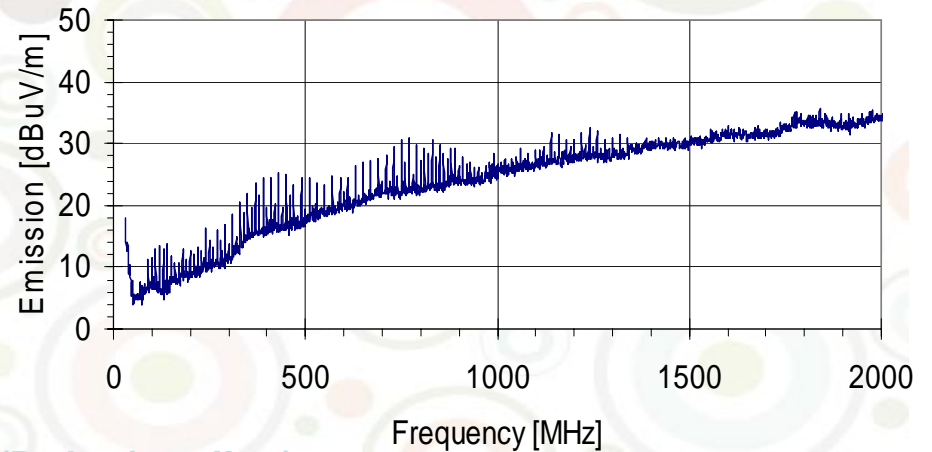


Reduction of CM radiation by embedded capacitors excited by short traces

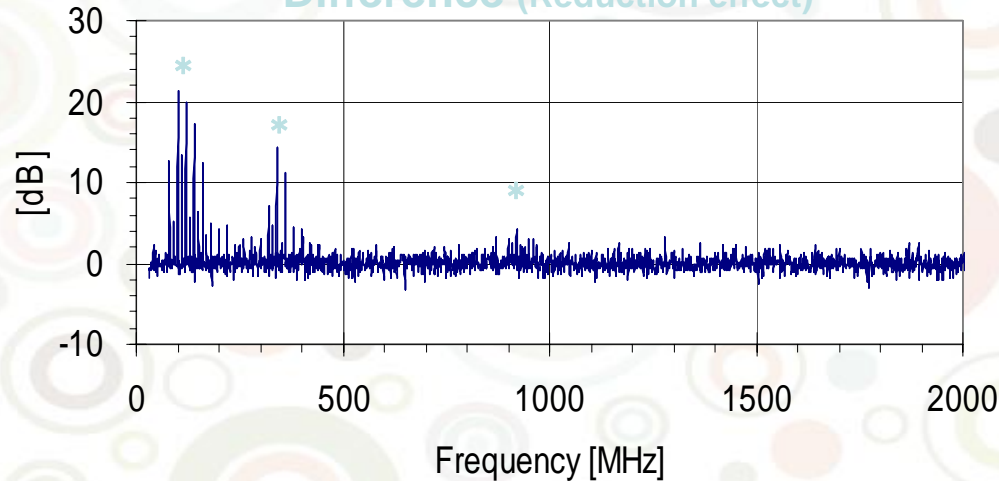
H= 200 um



H= 8 um



Difference (Reduction effect)



- CM radiation due to shoot-through current was significantly reduced by embedded capacitor. Reduction effect was almost same with long trace.

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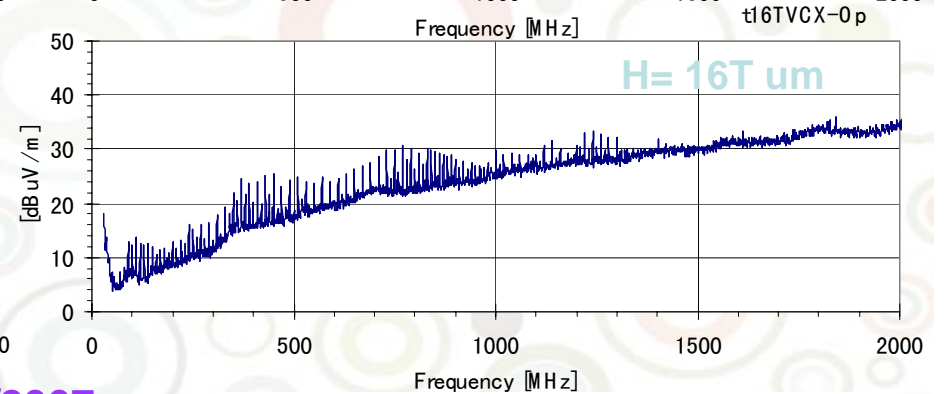
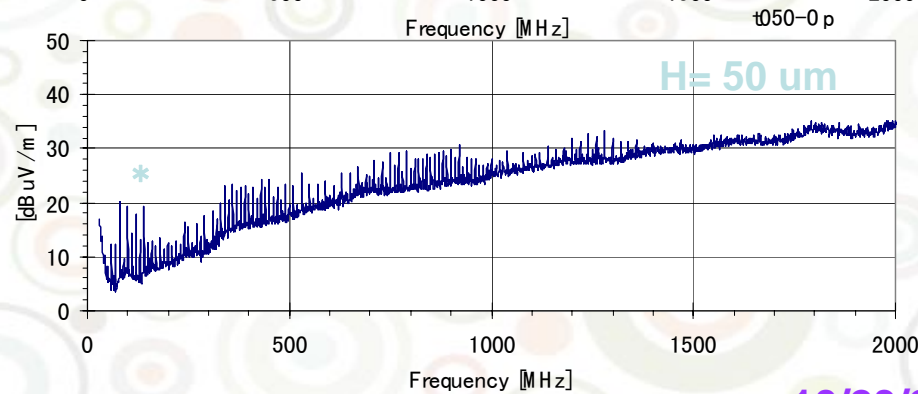
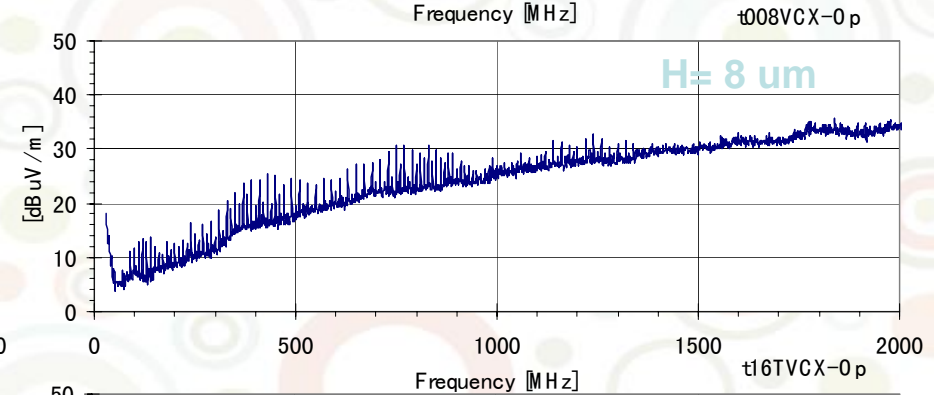
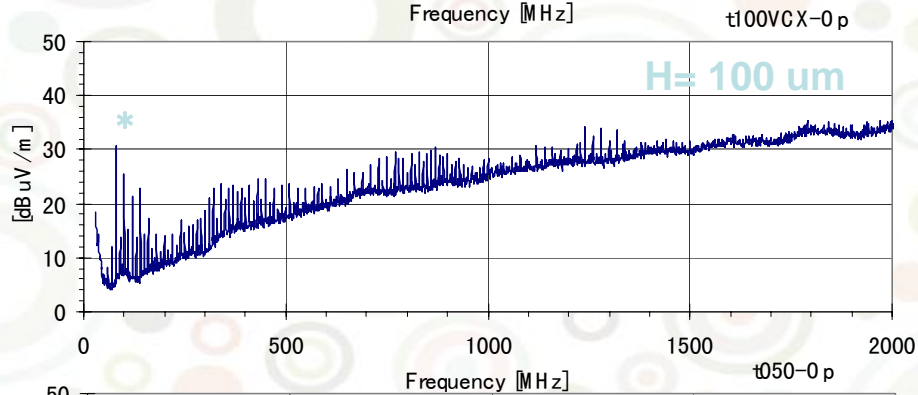
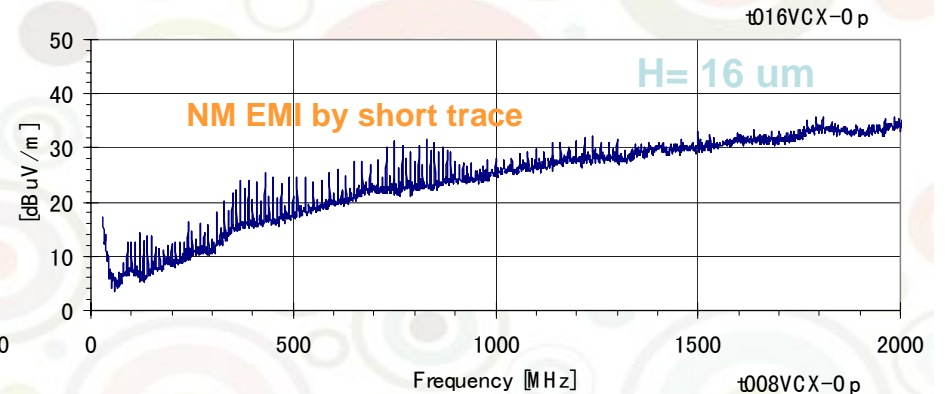
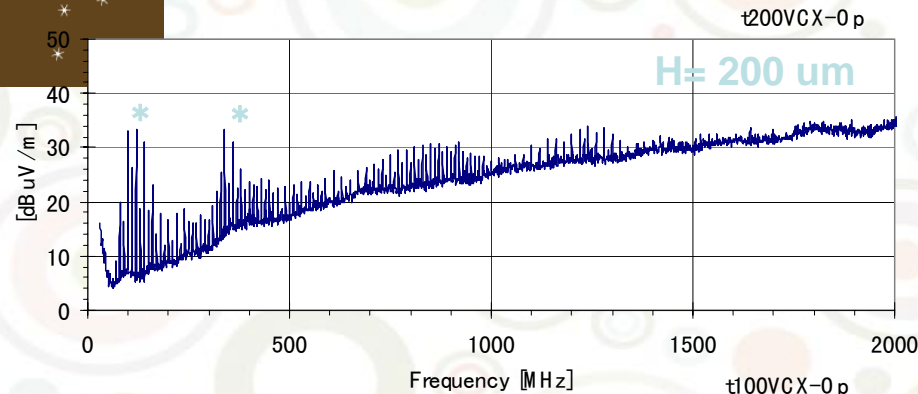
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CM radiated emission dependency on insulator thickness excited by short traces



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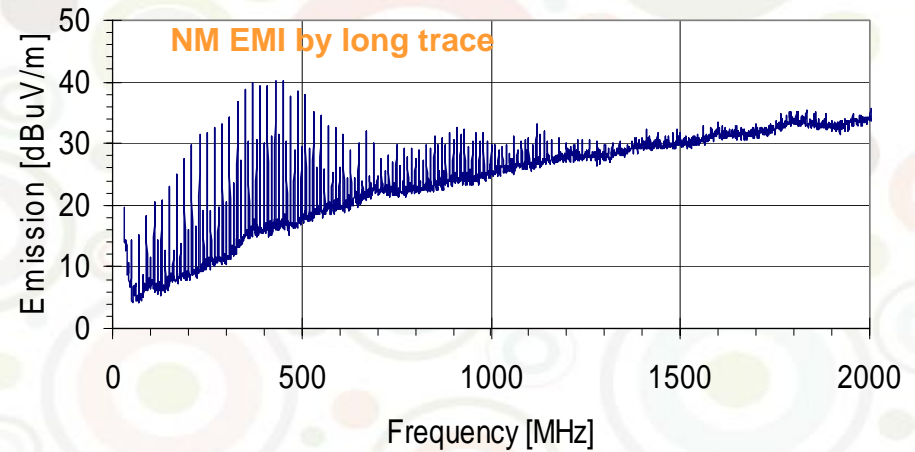
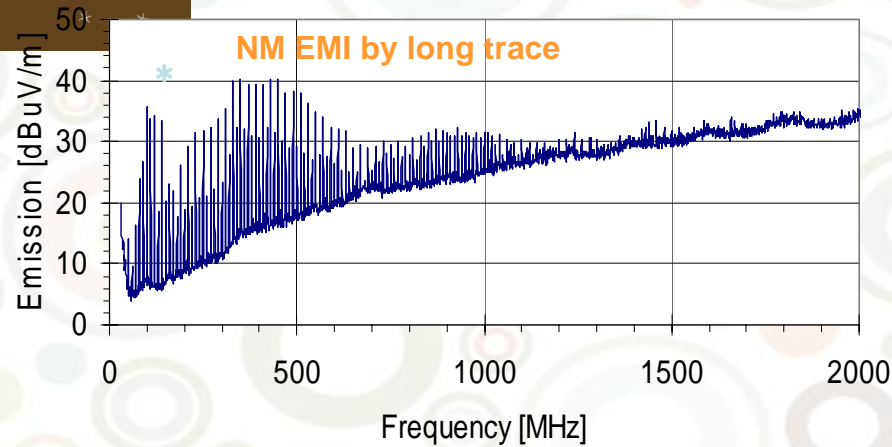




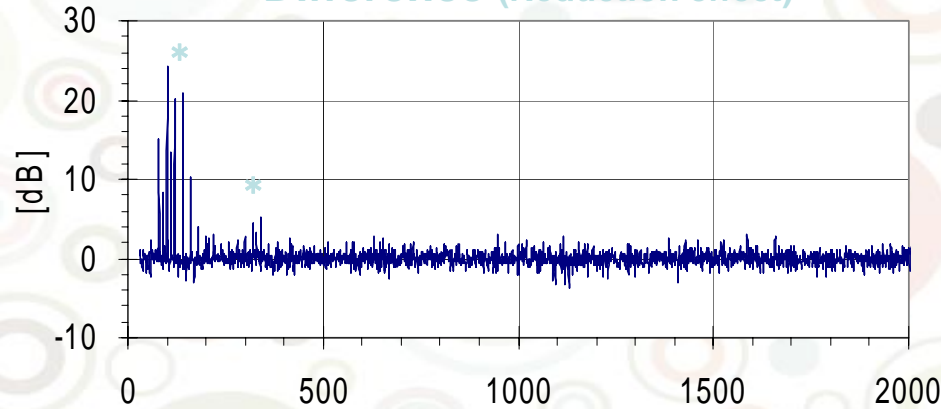
Radiated emission reduction by global capacitors excited by long traces H=200 um

Without global caps

With global caps



Difference (Reduction effect)



- Similar reduction effect was observed for the global capacitor, but frequency range was limited.

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Toshiba Summary

- 1) Power bus structure **with embedded decoupling capacitor** was characterized experimentally.
- 2) Low S21 property was obtained in a wide frequency range by the embedded decoupling capacitor **with thicknesses less than 16 um.**
- 3) **CM radiation due to shoot-through current** was significantly reduced in a wide frequency range by the embedded decoupling capacitor.
- 4) Global capacitors were effective for reducing EMI in a limited frequency range **with relatively thick insulators.**

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Project Team Formation

- (NCR) Teradata inquired about Buried Capacitance from Sanmina-SCI
- Sanmina contacted OMT about helping with evaluation
- Decided to form Project Team
 - Each would get commitment from Management
 - Each Member would supply the resources/materials for their part of the evaluation
 - Agreed to share results of evaluation
- TechDream brought into Team to provide simulation capability

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Team Members

Norm Smith (Teradata)
Jun Fan (Teradata/UMR)
Jim Knighten (Teradata)
John Andresakis (Oak-Mitsui Technologies)
Yoshi Fukawa (TechDream)
Mark Harvey (Sanmina-SCI)
Greg Schroeder (Sanmina-SCI-retired)

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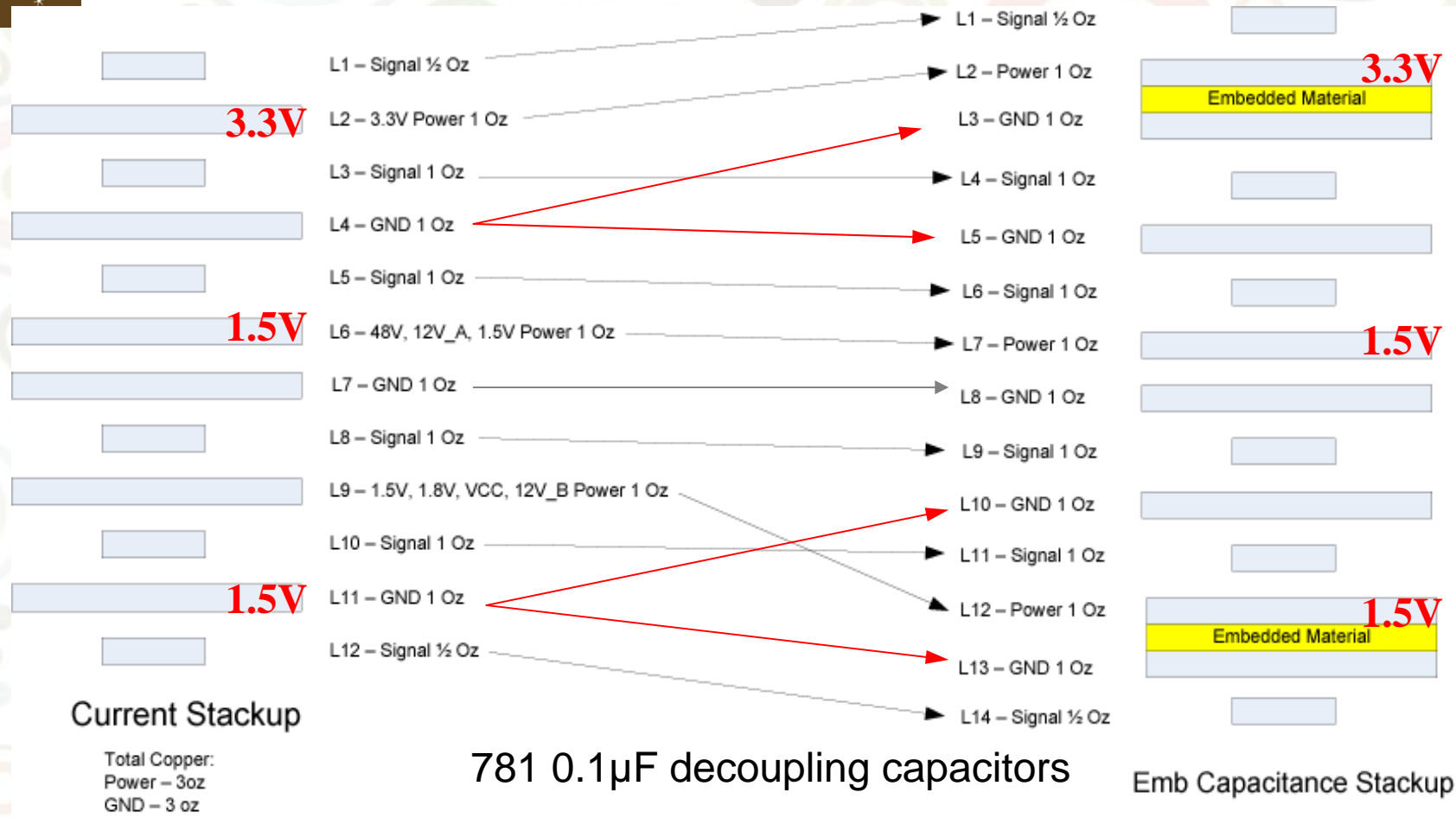
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Design Review



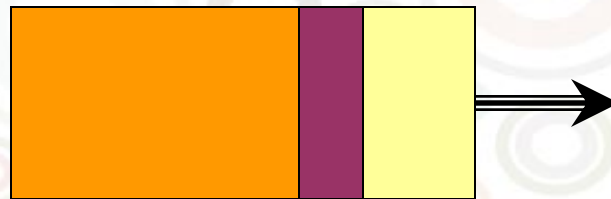
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Product Build

- No Process changes vs. Standard build
- Utilized BC24, BC12 (DK 4.4) and BC12TM (Dk 10)
- Leaders utilized for 12 μm cores



- High Potential (Hi-Pot) testing parameters adjusted versus 2 mil product (BC2000)
 - Lower Ramp Rate
 - Accounted for Charging vs. Leakage Current

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Electrical Performance

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Capacitance Measurements

(courtesy of Univ. of Missouri at Rolla)

Plane Pair	FR-4 (nF)	BC24 (nF)	BC12 (nF)	BC12TM (nF)
1.5V/GND	76.1 (75.8)	179.5 (179.0)	286.7 (266)	487 (478)
3.3V/GND	21.2 (21.2)	323.8 (321.3)	551 (541)	1148 (1082)

From LCR Meter

Extracted from VNA

Note: 1.5V plane is split resulting in smaller capacitor area

Replaces 78.1 μF of capacitance on standard board
(781 capacitors of 0.1 μF)

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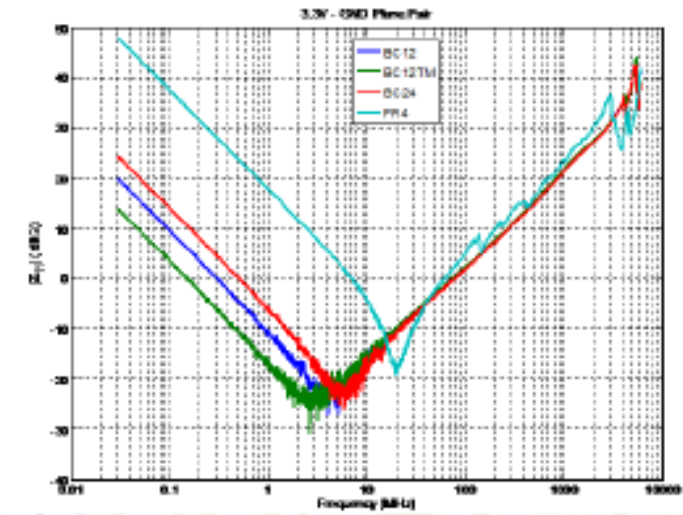
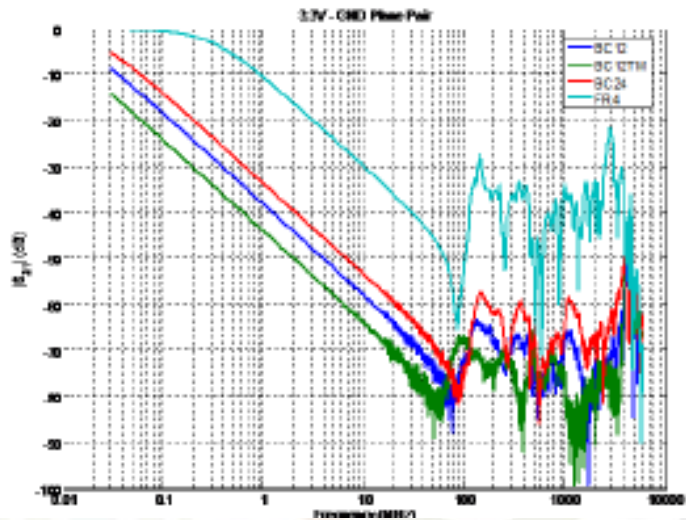
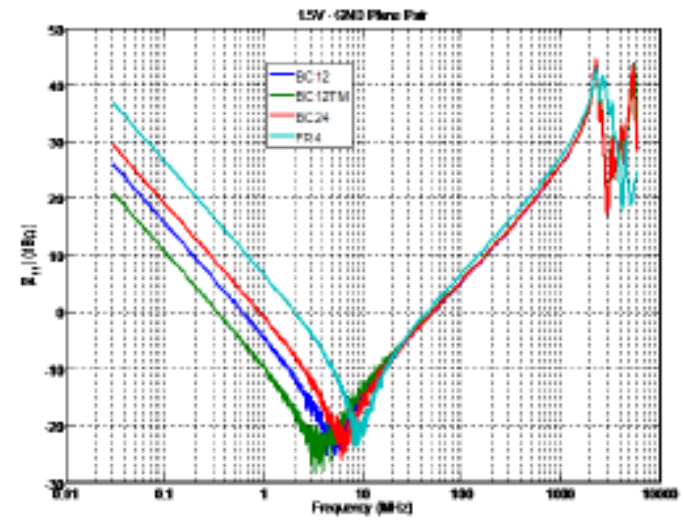
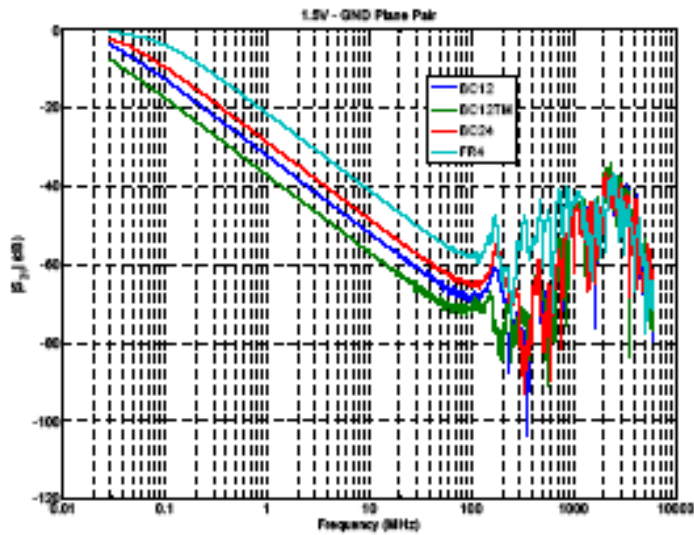




Board Impedance Measurements (S21, Z11)

Measurement Equipment : Agilent 8753D (Vector Network Analyzer)

Probe Point : Decoupling Capacitor Pad



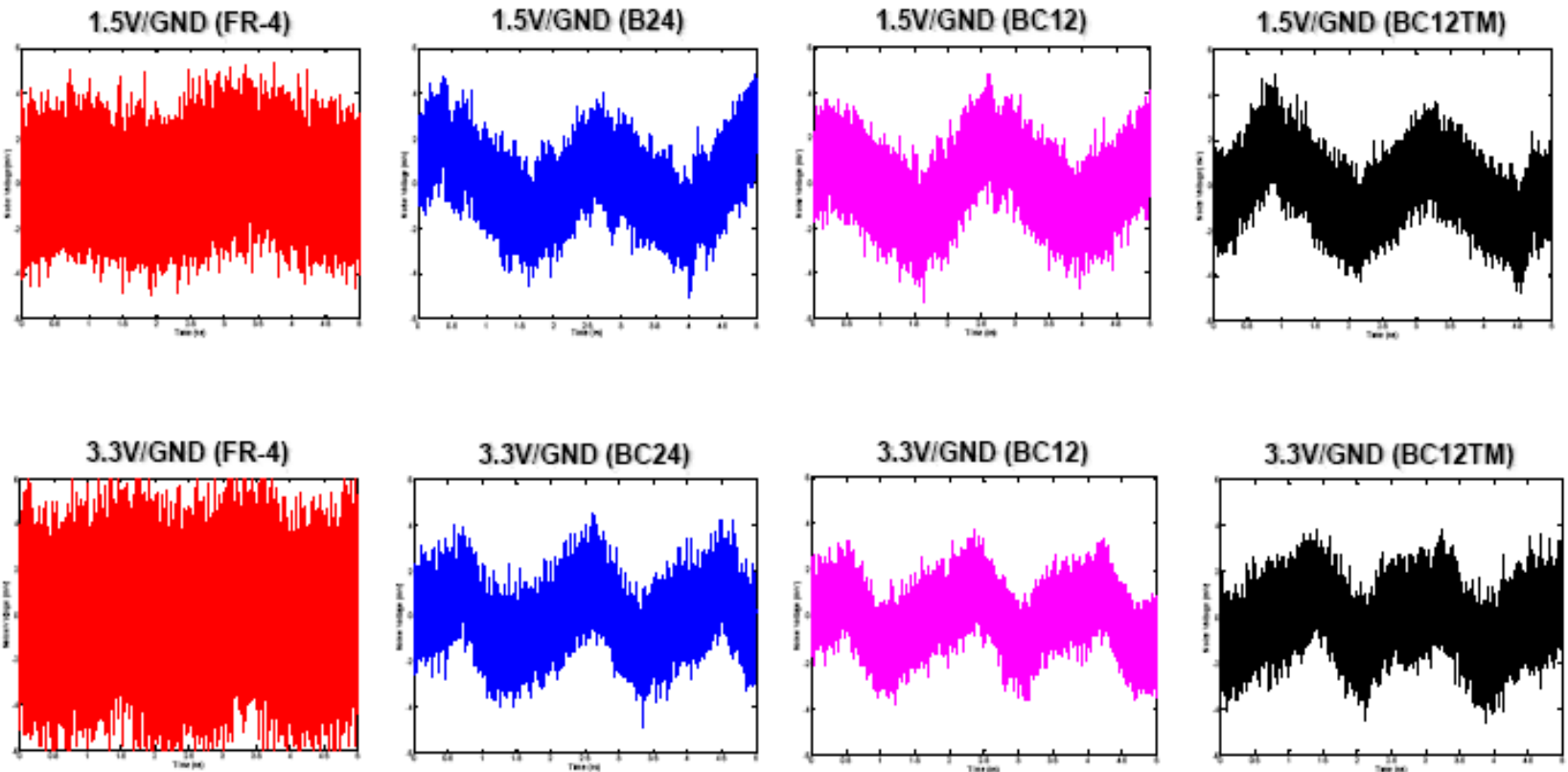
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Time Domain Power Bus Noise Measurement

Measurement Equipment : Agilent Infiniium 54855A (Digital Sampling Oscilloscope)

Probe Point : Decoupling Capacitor Pad



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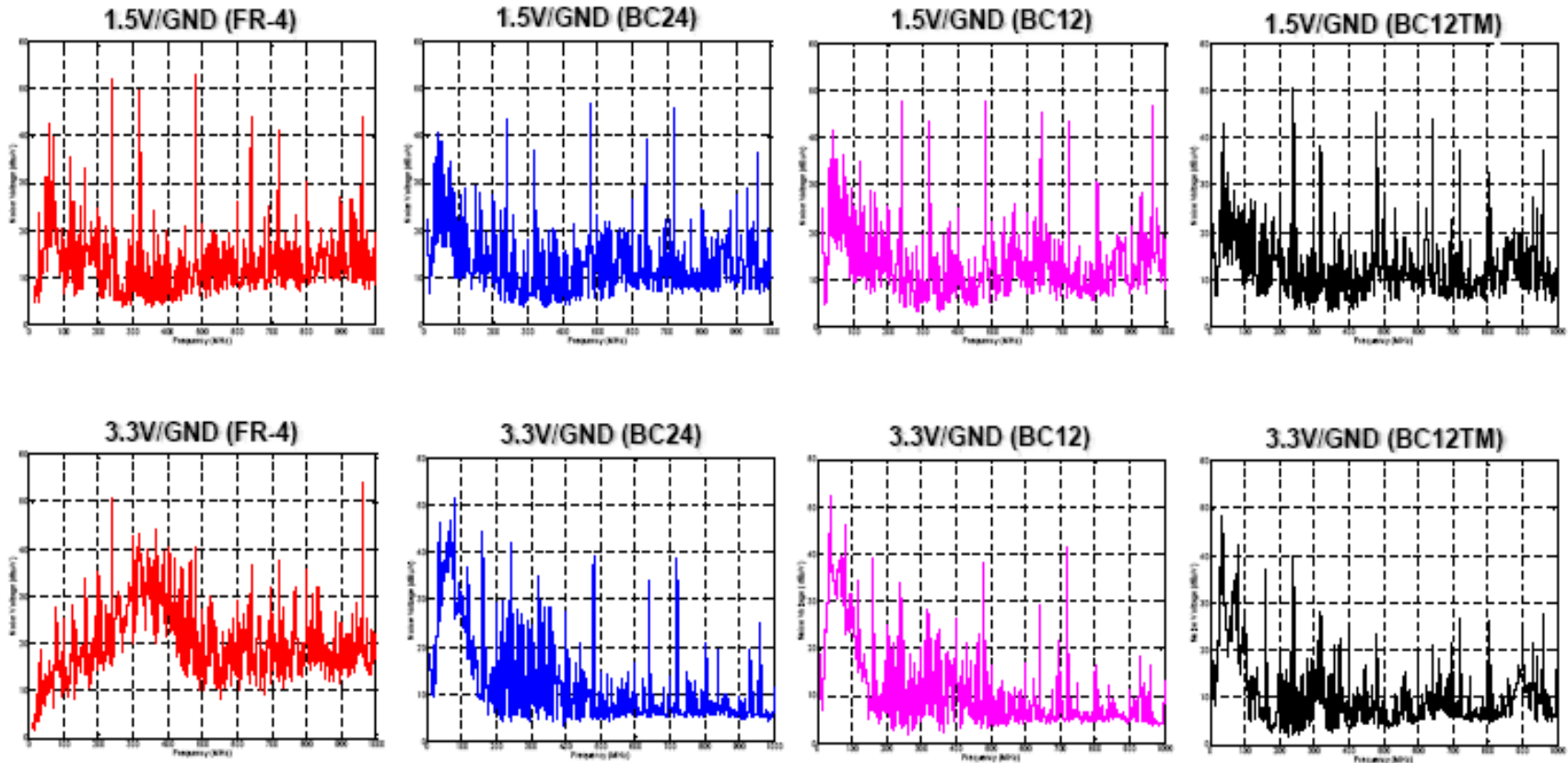


Frequency Domain Power Bus Noise Measurement

Measurement Equipment : Agilent E7404A (Spectrum Analyzer)

Tested to 1 GHz

Probe Point : Decoupling Capacitor Pad

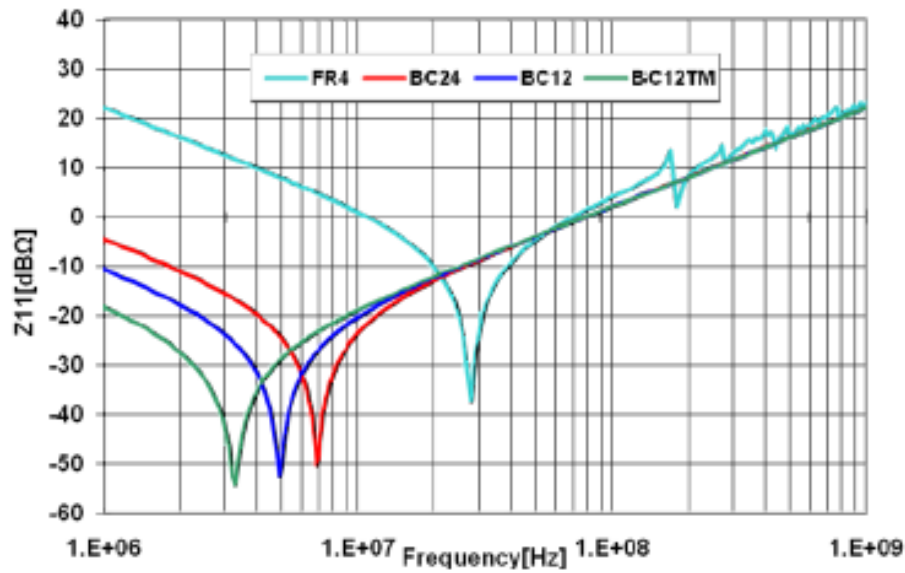


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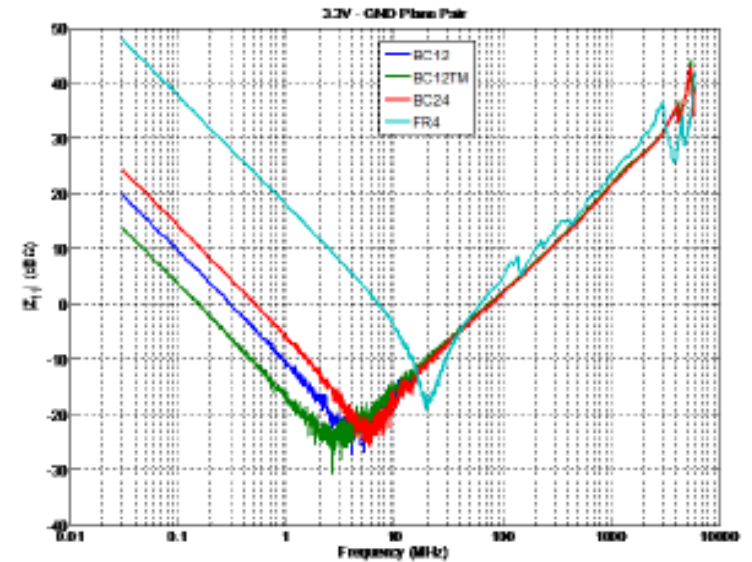


Simulation versus Measurements

EMISream Simulation



VNA Measurement



Very Good Correlation!!!

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Cost/Benefit Analysis

- **Cost Increases**
 - Layer Count went from 12 to 14
 - BC material cost increase vs. FR4
- **Cost Decrease**
 - 781 Decoupling Capacitors Eliminated

	12 to 14	Material
BC24	11.9%	5.1%
BC12	13.82%	10.43%
BC12TM	15.75%	19.25%

Based on low volume pricing

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Cost/Benefit Analysis

- Additional Benefits
 - 1562 vias eliminated (allows better routing, improves yields)
 - Increased reliability (1562 solder joints eliminated)
 - Better Performance at Higher Frequencies (reduced time to market)
 - Reduced EMI (less shielding required)
 - Possible size reduction and/or increased functionality

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Future Studies

- Measure actual EMI of the assembled board
- Measure Eye Diagrams
- Environmental testing of boards
- Determine product candidates to implement BC

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Lessons Learned

- Team approach using supply chain is effective in implementing new technology
- Projects will take longer than expected
 - Restart of some boards due to broken drill bits
 - Assembly took longer due to priority issues
- Designers must be willing to look at PDN in a different way (simulation assists in this effort).
- Manufacturing using BC materials is relatively easy to implement

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Summary

- Team formed between members of supply chain with commitment from Management
- 3 types of material picked to characterize effect of thickness and Dk
- Boards with BC layers, without all 781 decoupling capacitors, performed as good or better than standard board
- Simulation compared favorably to actual results
- Cost/Benefit of Buried Capacitance is extremely design dependant
- 24 μm had best cost performance for this design
- Initial BC Design will not typically utilize all the benefits of the technology.

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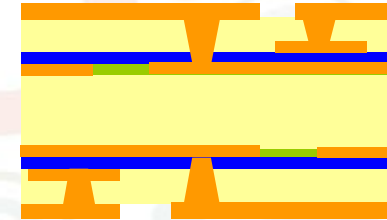
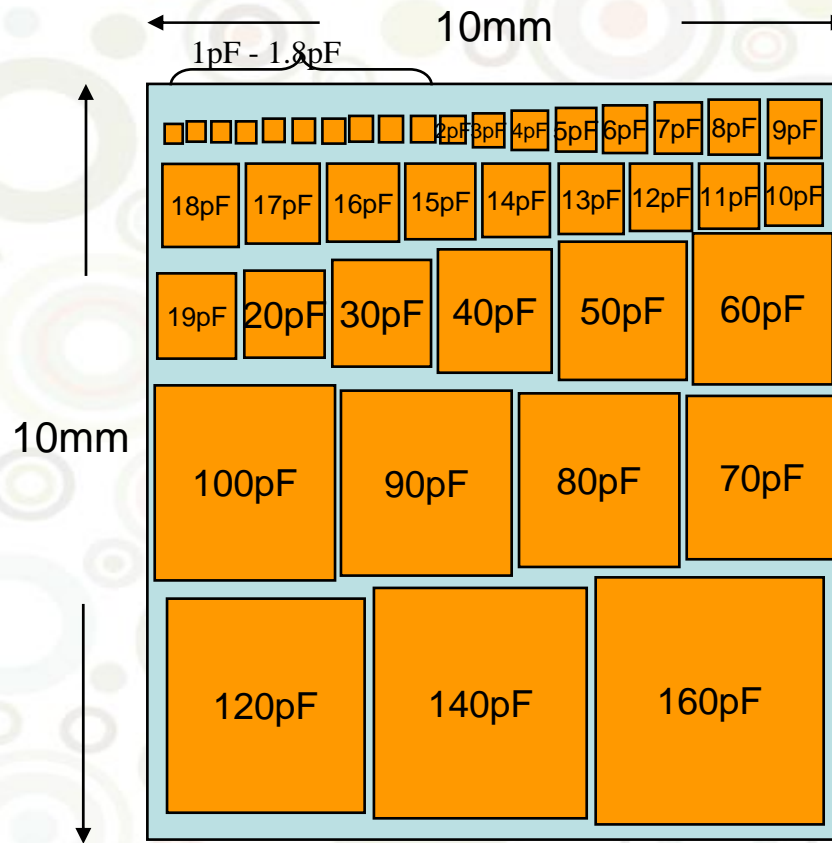
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Designing Embedded Capacitance Board Geometry and Capacitance(Example)

40 capacitors ranging from 1pF to 160pF in 10x10mm



Expected tolerance*

- 1 - 2pF 5 - 10%
- 2 - 10pF 3 - 5%
- 10 - 20pF 2 - 3%
- 20 - 100pF 1 - 2%
- 100 - < 1%

*Based on electrode geometry definition
+/- 10micron

Geometry calculated based upon
16μ Filled material: 1,700pF/cm²

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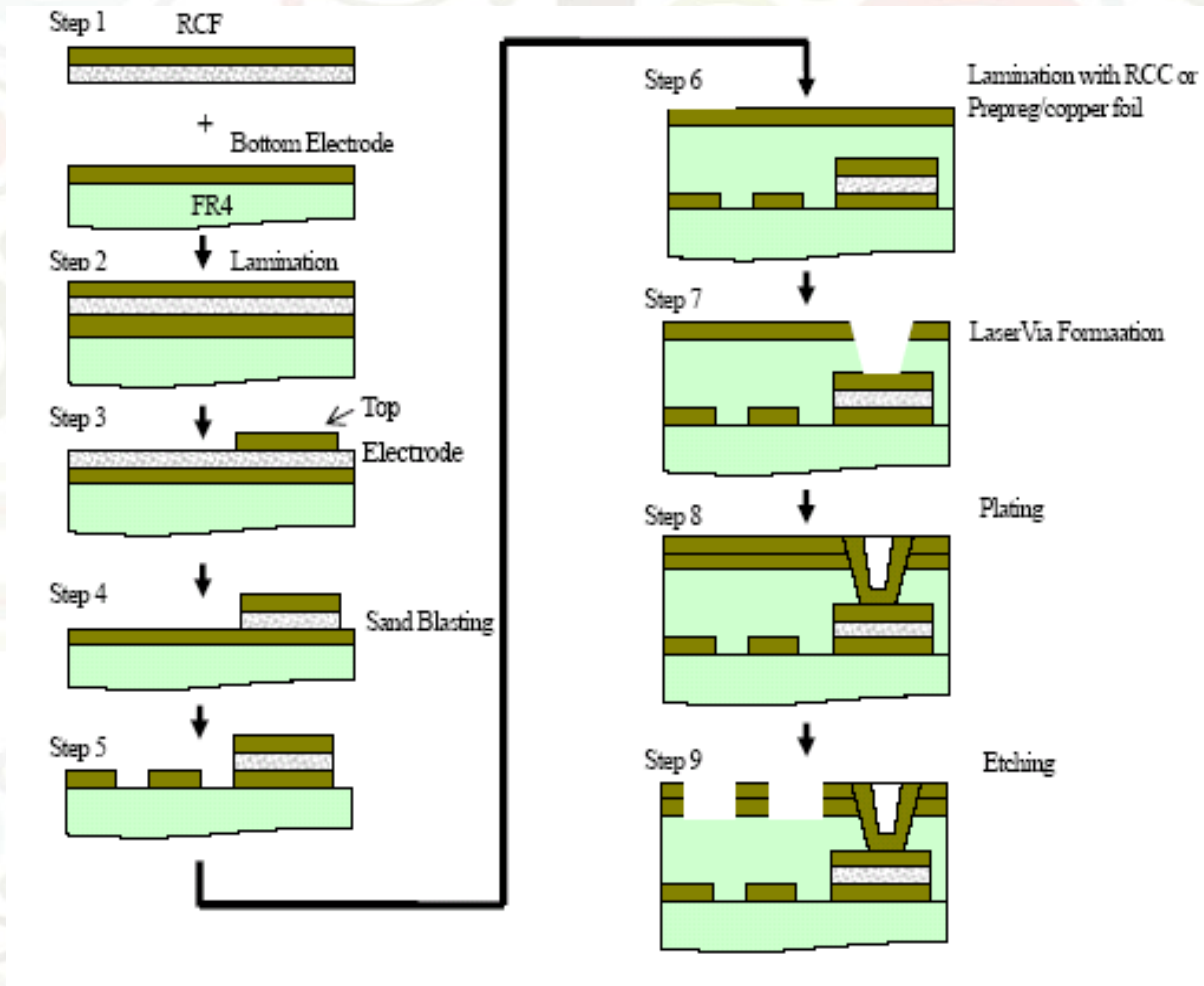
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“Discrete” Capacitor Process Using Resin Coated Foil



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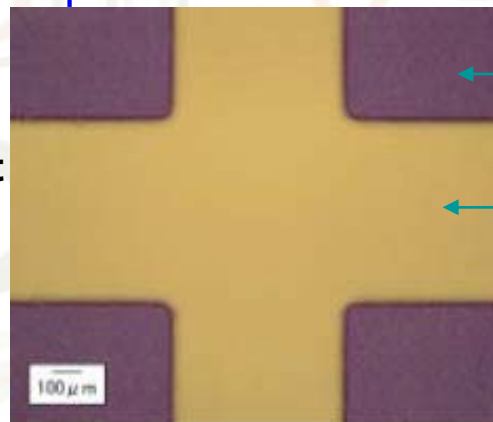


Removal of dielectric layer

Top view

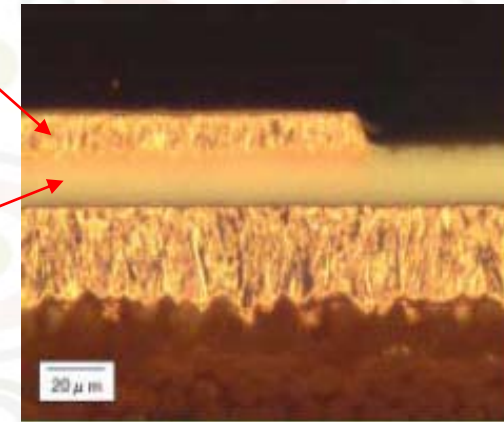
Cross sectional

Before sand blast process

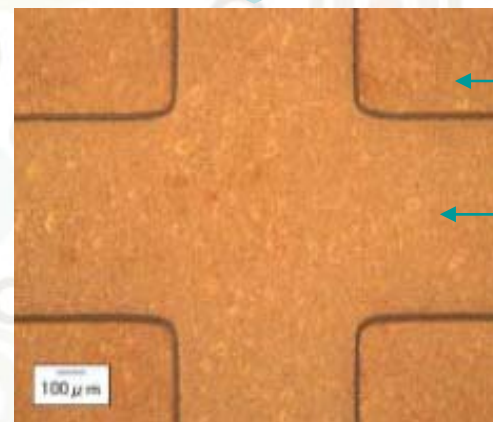


Top electrode

Dielectric layer

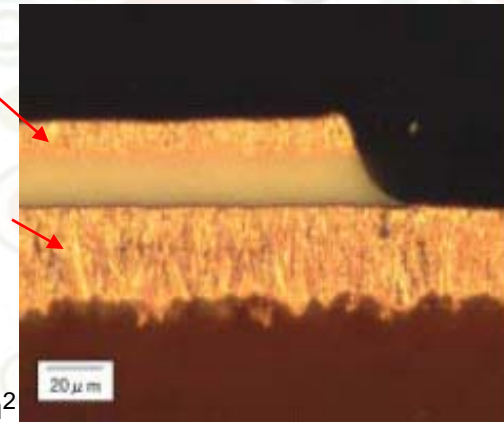


After sand blast process



Top electrode

Bottom electrode



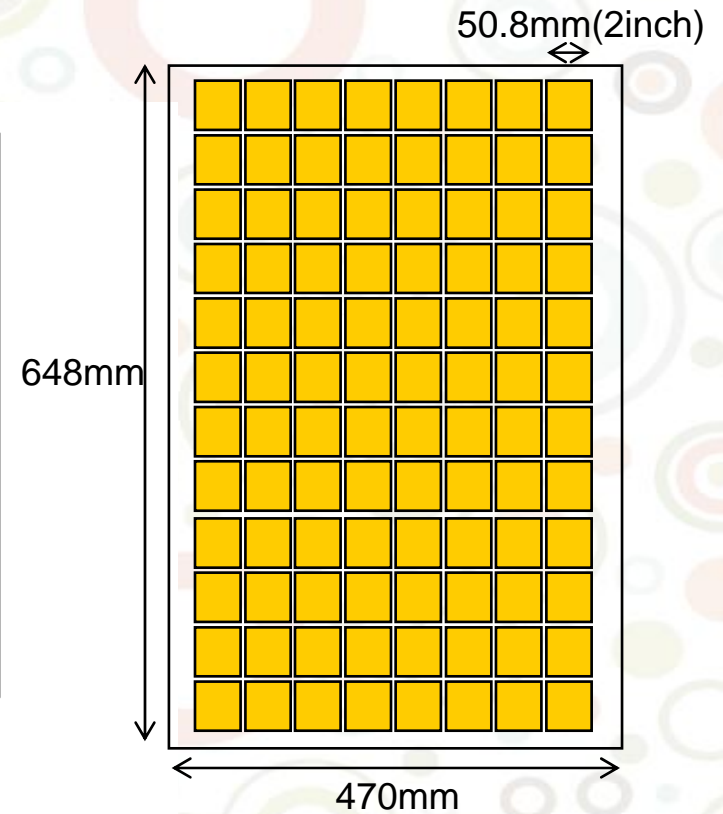
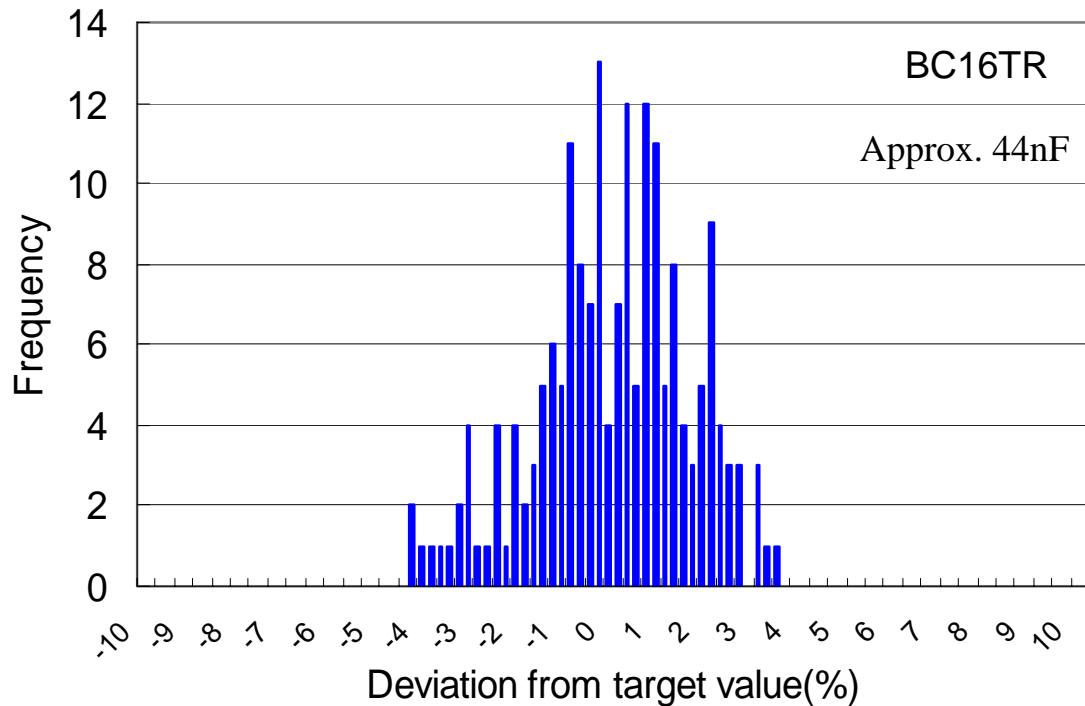
Ishi Hyoki
#A600, 5kg/cm²

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Capacitance uniformity evaluation result

Test 1.



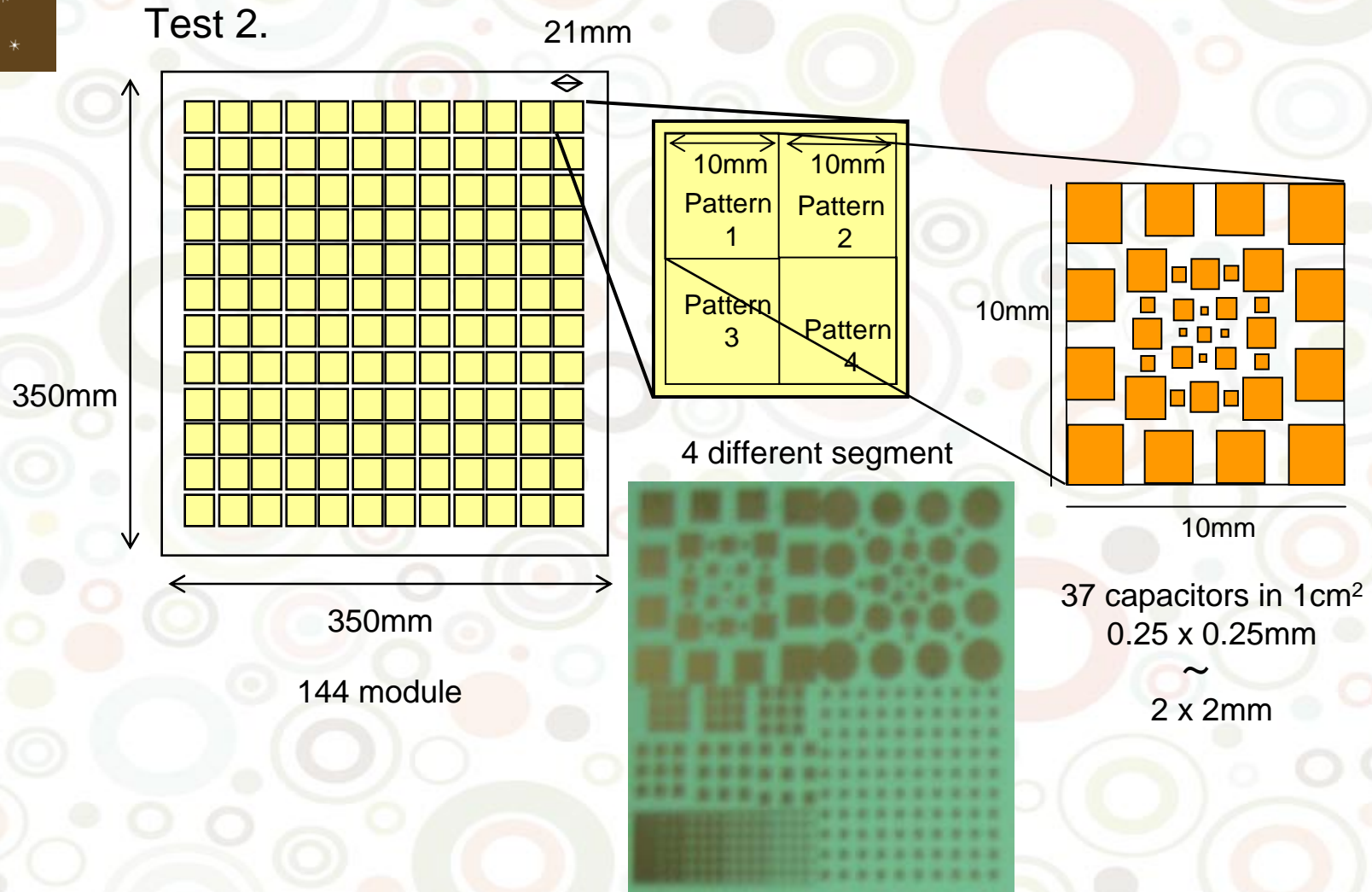
Capacitor size : 50.8x50.8mm
192 measurement points

Uniformity <5%

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Capacitance uniformity evaluation



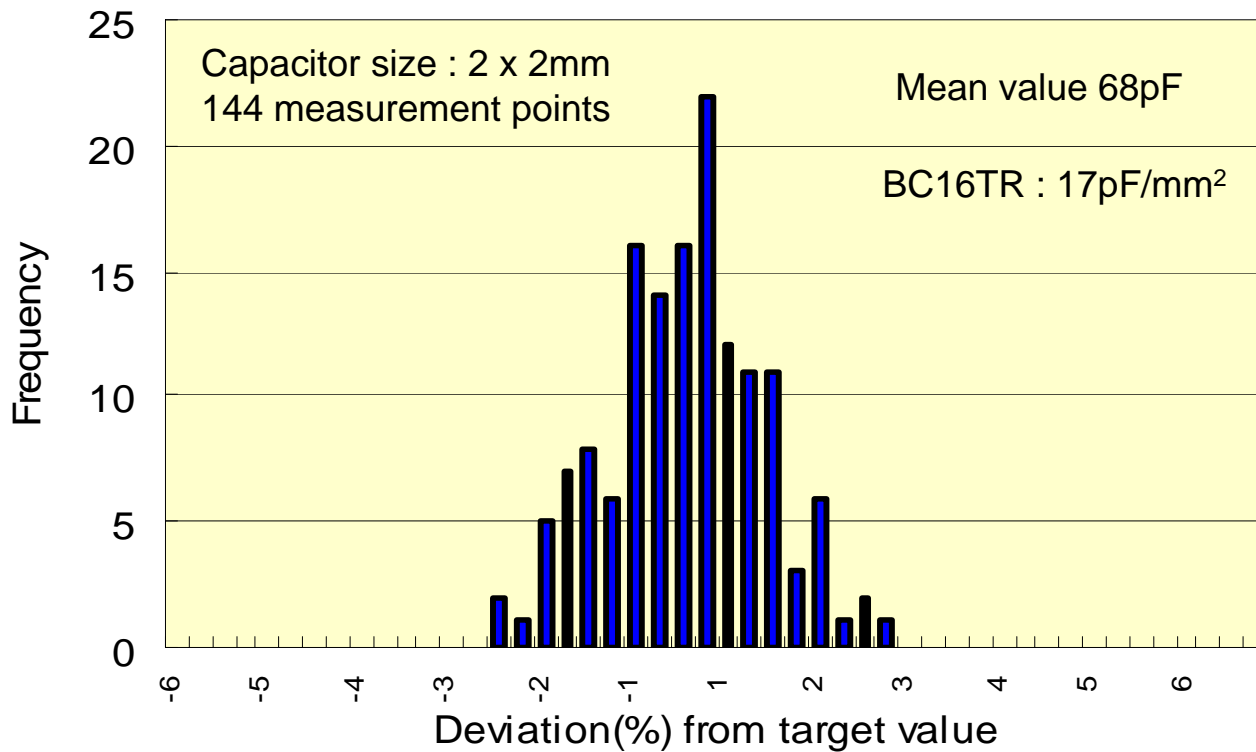
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Capacitance uniformity evaluation result

Test 2.

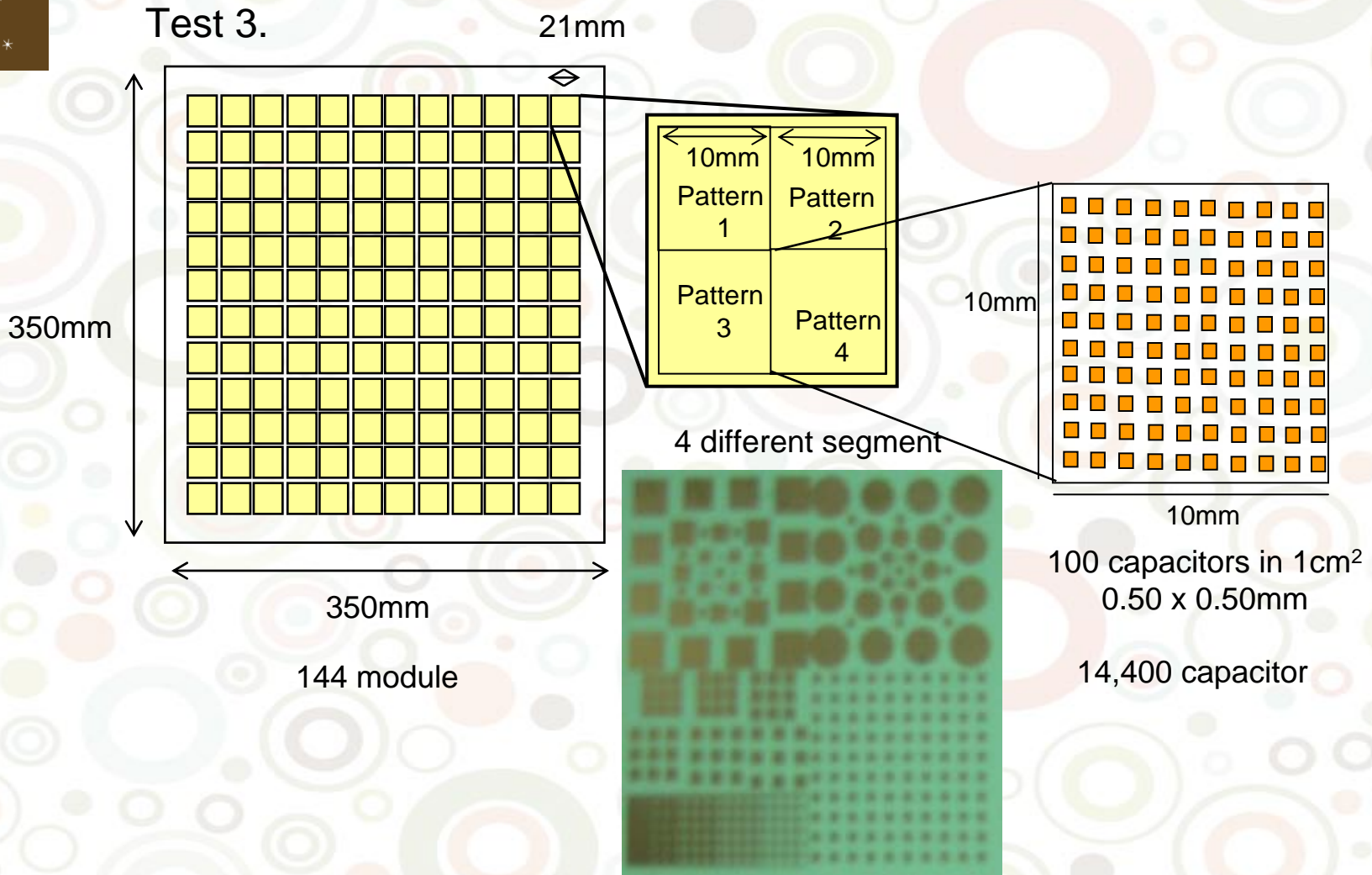


Uniformity <5%

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Capacitance uniformity evaluation



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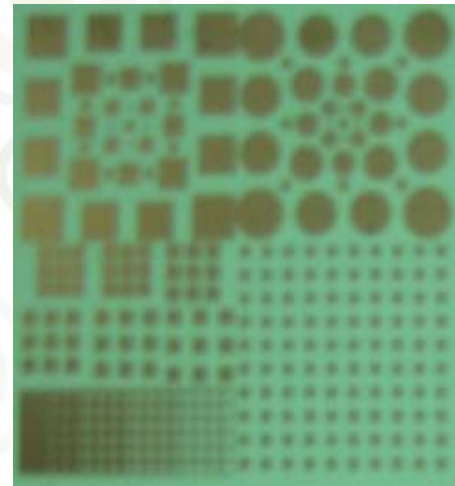
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Flying probe LCR measurement of embedded passive Boards



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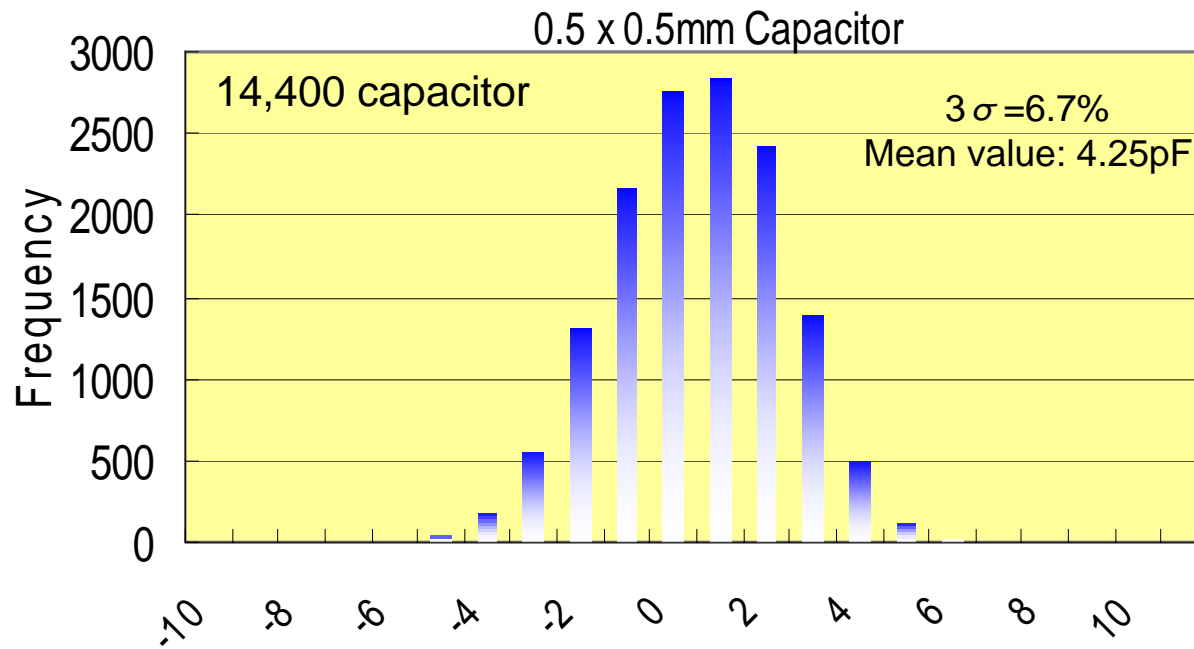
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Capacitance uniformity evaluation result

Test 3.



Variation from mean value

Uniformity <7%

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Discrete Capacitor Summary

- Manufactured using HDI Processing
- +/- 10% tolerance is achievable
- X7R TCC Capable
- Recommend for Lower Voltage Applications (under 15 volts)
 - Electro-migration tested to 1000 hours (85%/85°C)
- Available from several suppliers

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Thank You

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